

Peta-Flop Radio Astronomy Signal Processing and the CASPER Collaboration (and correlators too !)

Dan Werthimer and 800 CASPER Collaborators

<http://casper.berkeley.edu>



Two Types of Signal Processing

1. Embarrassingly Parallel – Low Data Rates

(record the data and process it later)

(high computation per bit)

2. Real Time in-situ Processing

Petabits per second (can not record data)

TYPE 1

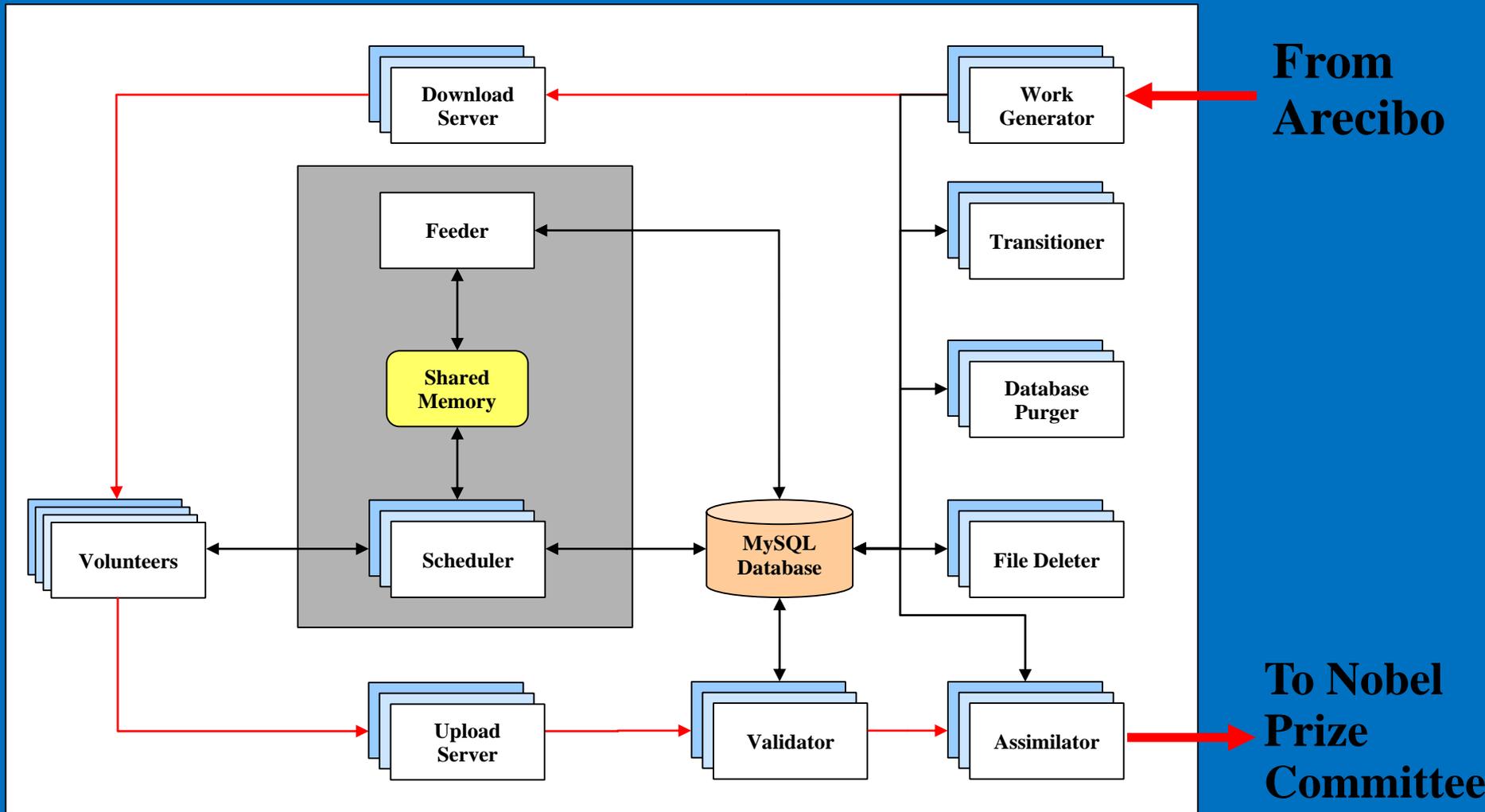
Embarrassingly Parallel – Low Data Rates

(record the data and process it later)

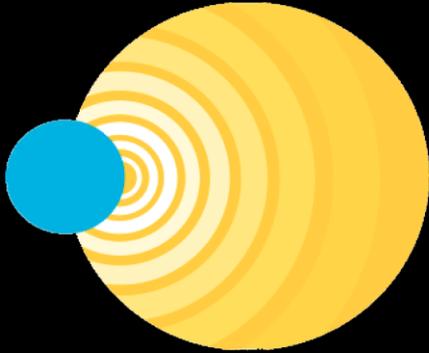
(high computation per bit)

VOLUNTEER COMPUTING

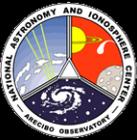
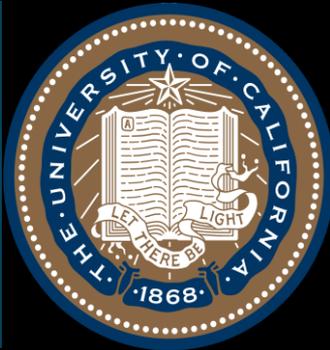
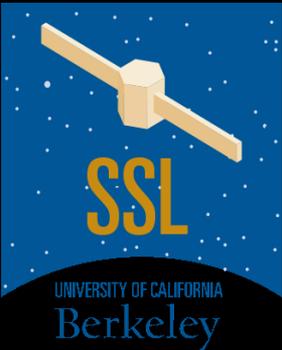
BOINC - Berkeley Open Infrastructure for Network Computing



BERKELEY SETI RESEARCH CENTER



BERKELEY SETI



Berkeley SETI and Volunteer Computing Group

David Anderson, Hong Chen, Jeff Cobb, Matt Dexter,
Walt Fitelson, Eric Korpela, Matt Lebofsky, Geoff Marcy,
David MacMahon, Eric Petigura, Andrew Siemion,
Charlie Townes, Mark Wagner, Ed Wishnow, Dan Werthimer

NSF , NASA, Individual Donors

Agilent, Fujitsu, HP, Intel, Xilinx





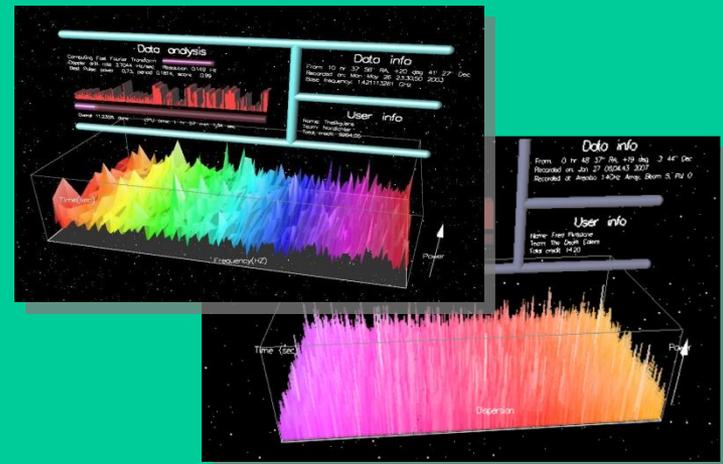
Arecibo Observatory



High performance data storage silo

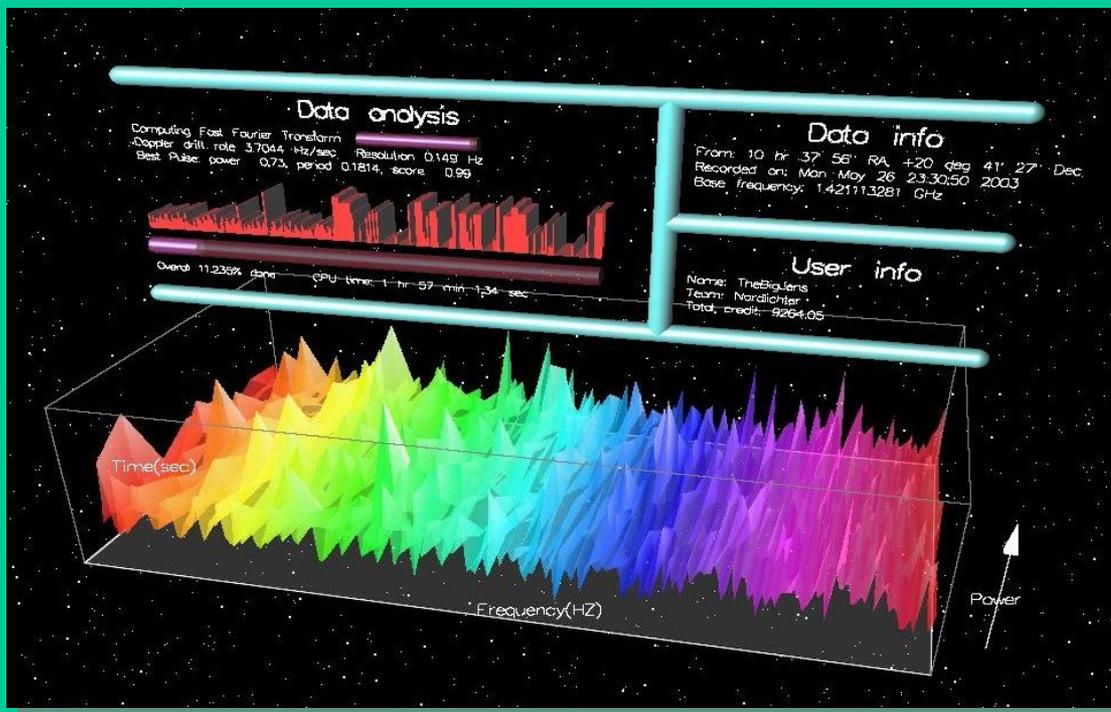


UC Berkeley Space Sciences Lab



Public Volunteers

SETI@Home



- * Polyphase Channelization
- * Coherent Doppler Drift Search
- * Narrowband Pulse Search
- * Gaussian Drift Search
- * Autocorrelation
- * <insert your algorithm here>

SETI@home Statistics

TOTAL

RATE

8,464,550
participants
(in 226 countries)

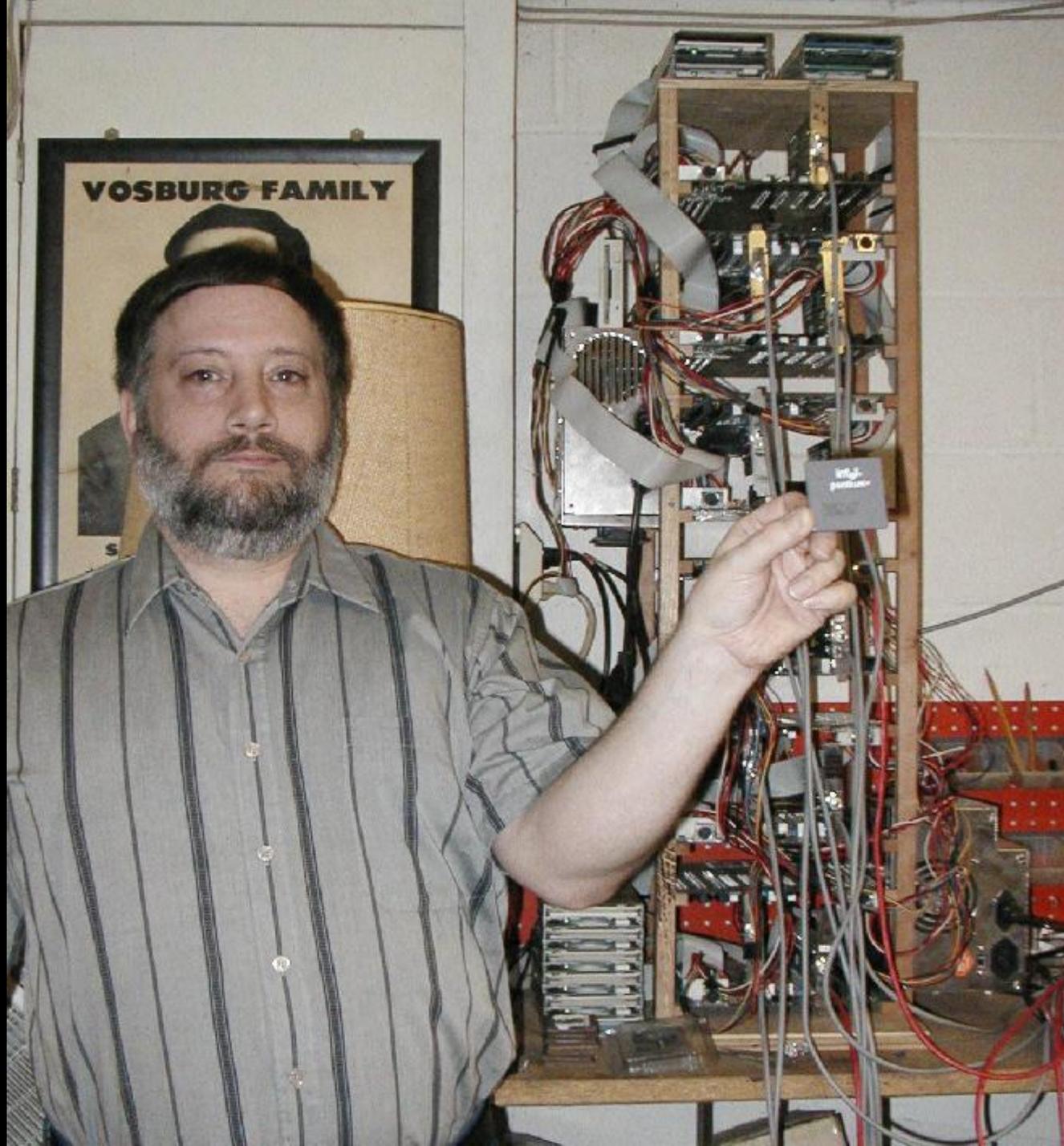
2,000 per day

3 million years
computer time

1,000 years per day

$3 * 10^{23}$
operations

3,000 Tera-flops





Projects

- Astronomy
 - SETI@home (Berkeley)
 - Astropulse (Berkeley)
 - Einstein@home: gravitational pulsar search (Caltech,...)
 - PlanetQuest (SETI Institute)
 - Stardust@home (Berkeley, Univ. Washinton,...)
- Earth science
 - Climateprediction.net (Oxford)
- Biology/Medicine
 - Folding@home, Predictor@home (Stanford, Scripts)
 - FightAIDSathome: virtual drug discovery
- Physics
 - LHC@home (Cern)
- Other
 - Web indexing/search
 - Internet Resource mapping (UC Berkeley)

Data analysis

Searching for Pulses / Targets
 Doppler shift rate 0.0000 Hz/sec Resolution 1220.703 Hz
 New Pulses power 0.33 period 0.1334 score 0.53



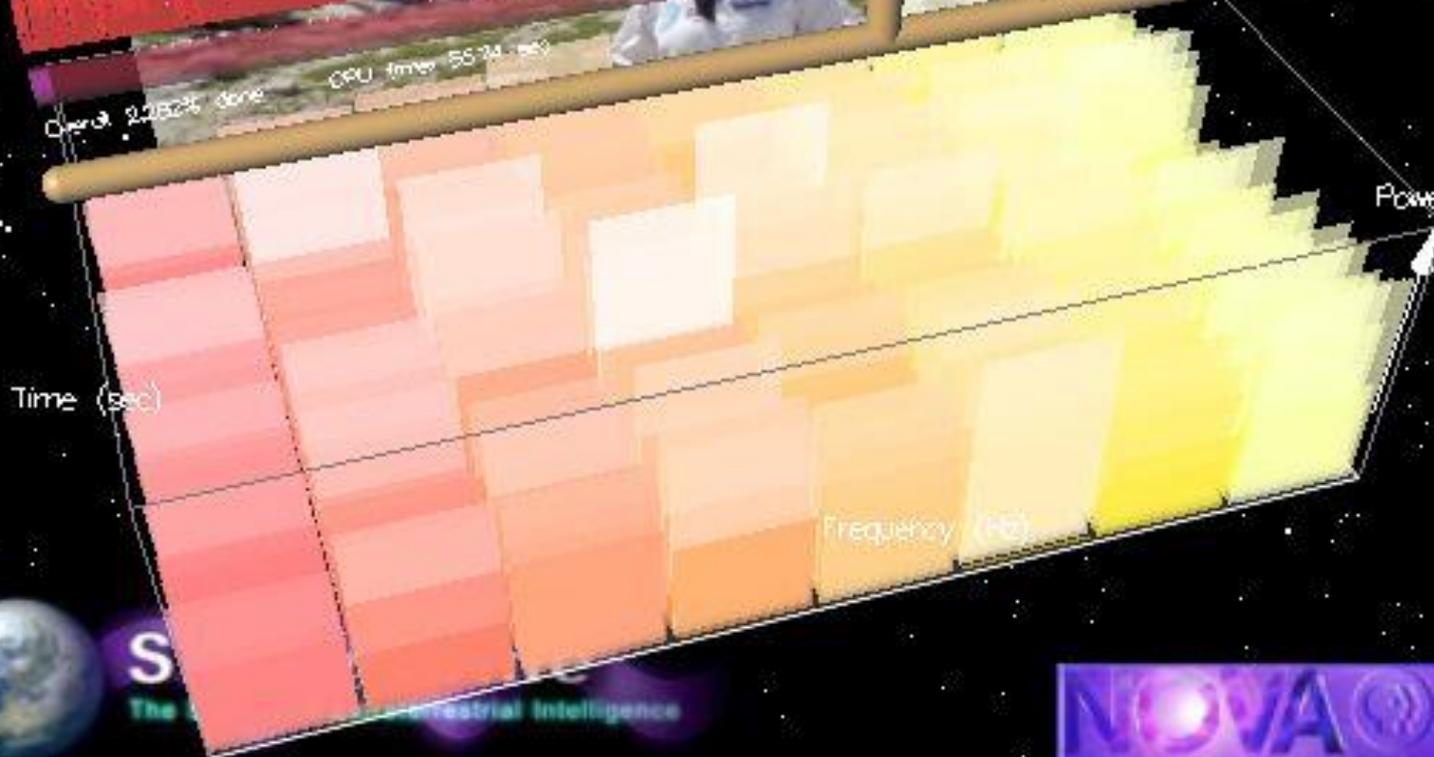
Chans 22524 done CPU time 55.34 sec

Data info

From 17 hr 42' 2" RA +19 deg 10' 59" Dec
 recorded on Tue Mar 02 12:08:44 2004
 Base frequency 1414236281 GHz

User info

Name David
 Email david@...
 IP 10.0.0.10

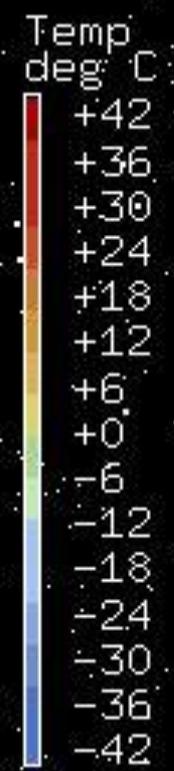
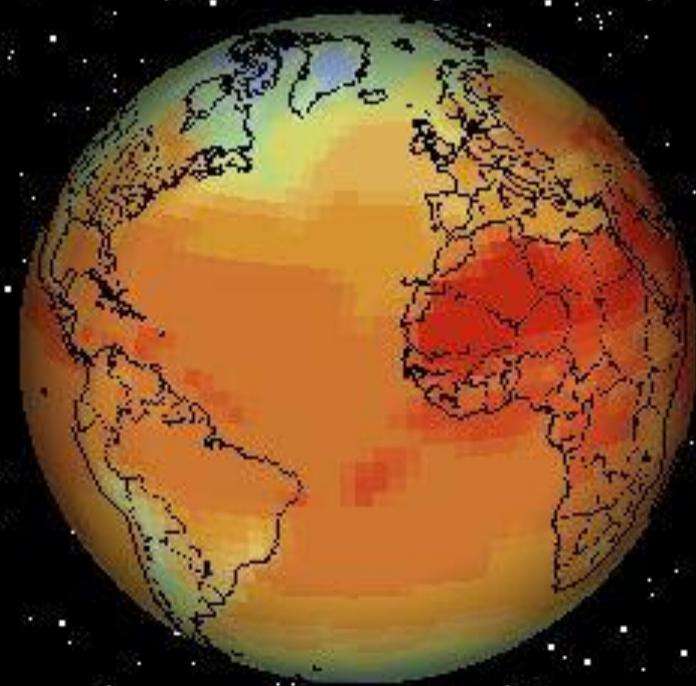


S

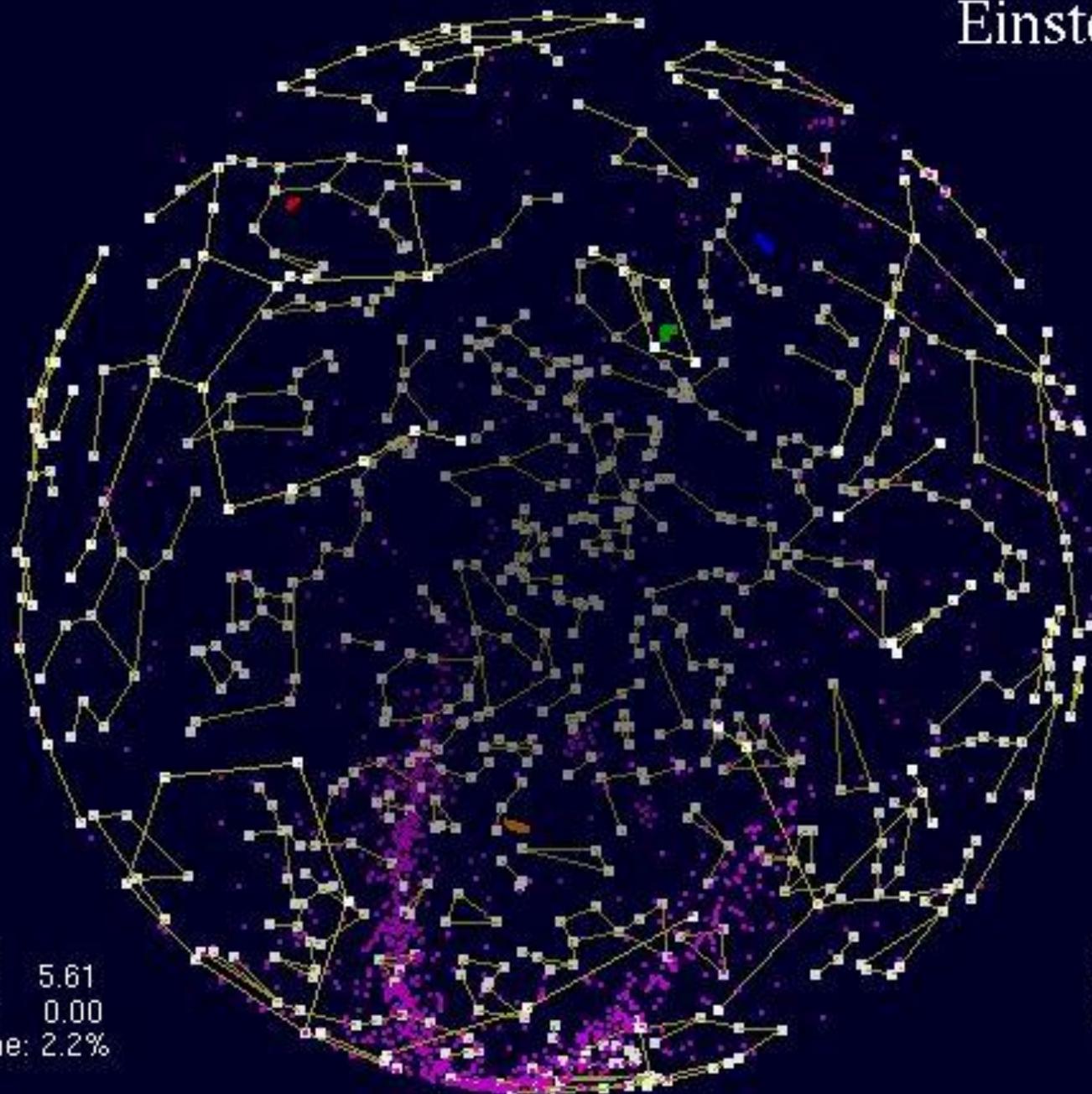
The ... Industrial Intelligence



climateprediction.net



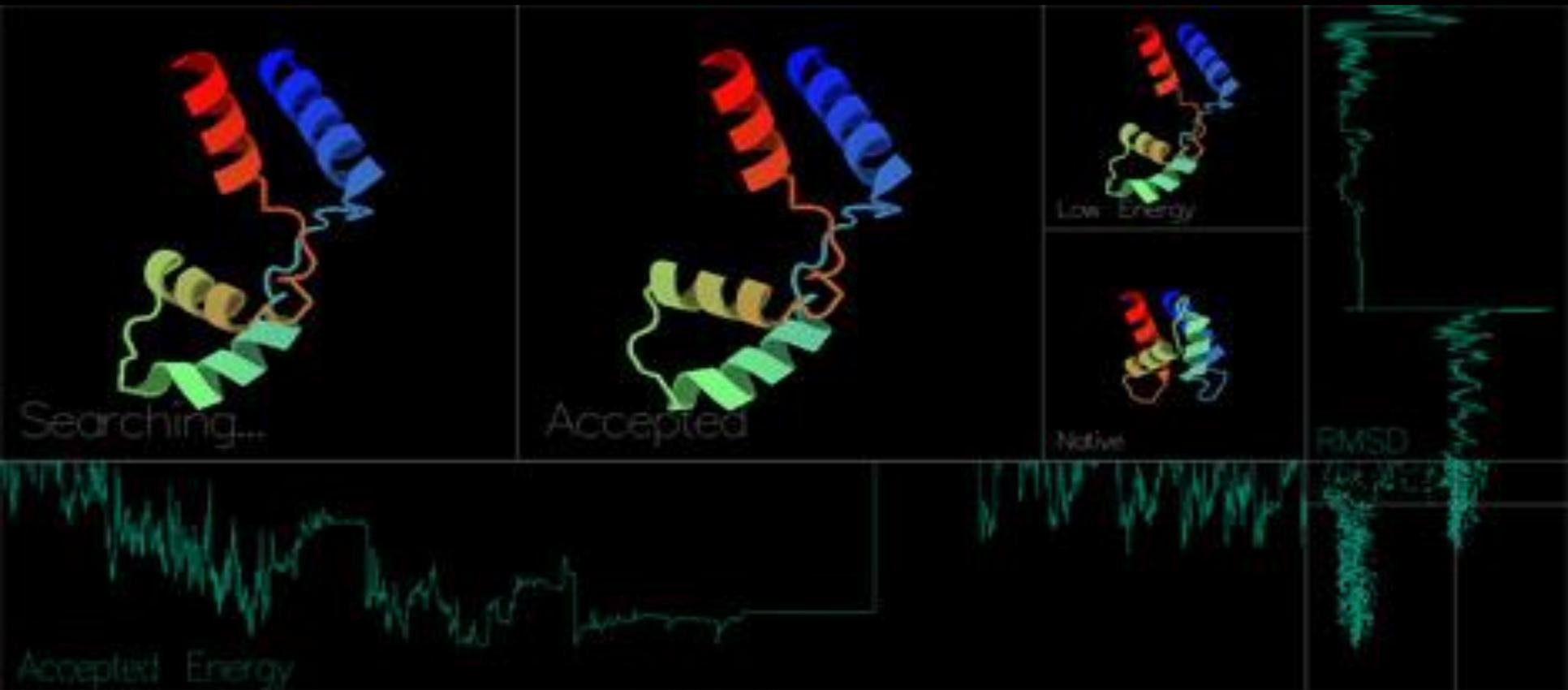
```
hads3  
User : David Anderson; Team : <None>  
Phase : 1 of 3 / Timestep : 25369 of 259248  
Model Date : 19/05/1812 12:30  
Run ID: 259r_100121161, CPU Time: 0025:22:35 (3.60 s/TS)  
T=Temp, F=Precip, R=Pressure, S=SmoothCld, U=GridCld
```



User: davea
Total Credit: 5.61
Host Credit: 0.00
Percent Done: 2.2%

Search Position
RA: 172.30
DEC: -83.12

Rosetta Screensaver

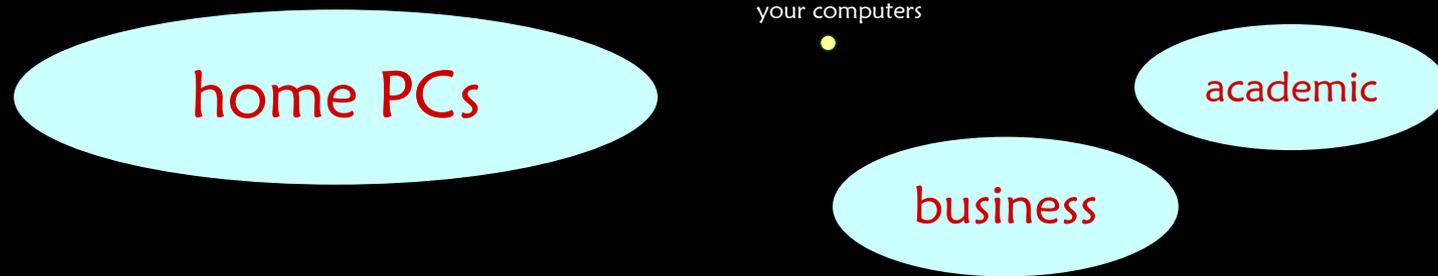


Modeling the calcium sensitive switching behavior of S100A.

72.04% Complete
CPU time: 4 hr 19 min 24 sec
Michael G.R. - Total credit: 58695.5 - PAC: 288.155
betterhumans.com
Rosetta@home v5.59 <http://boinc.bakerlab.org/rosetta/>

Stage: Relax
Model: 24 Step: 21-212
Accepted RMSD: 14.43
Accepted Energy: -3885603

Where's the computing power?



2010: 1 billion Internet-connected PCs

55% privately owned

If 100M participate:

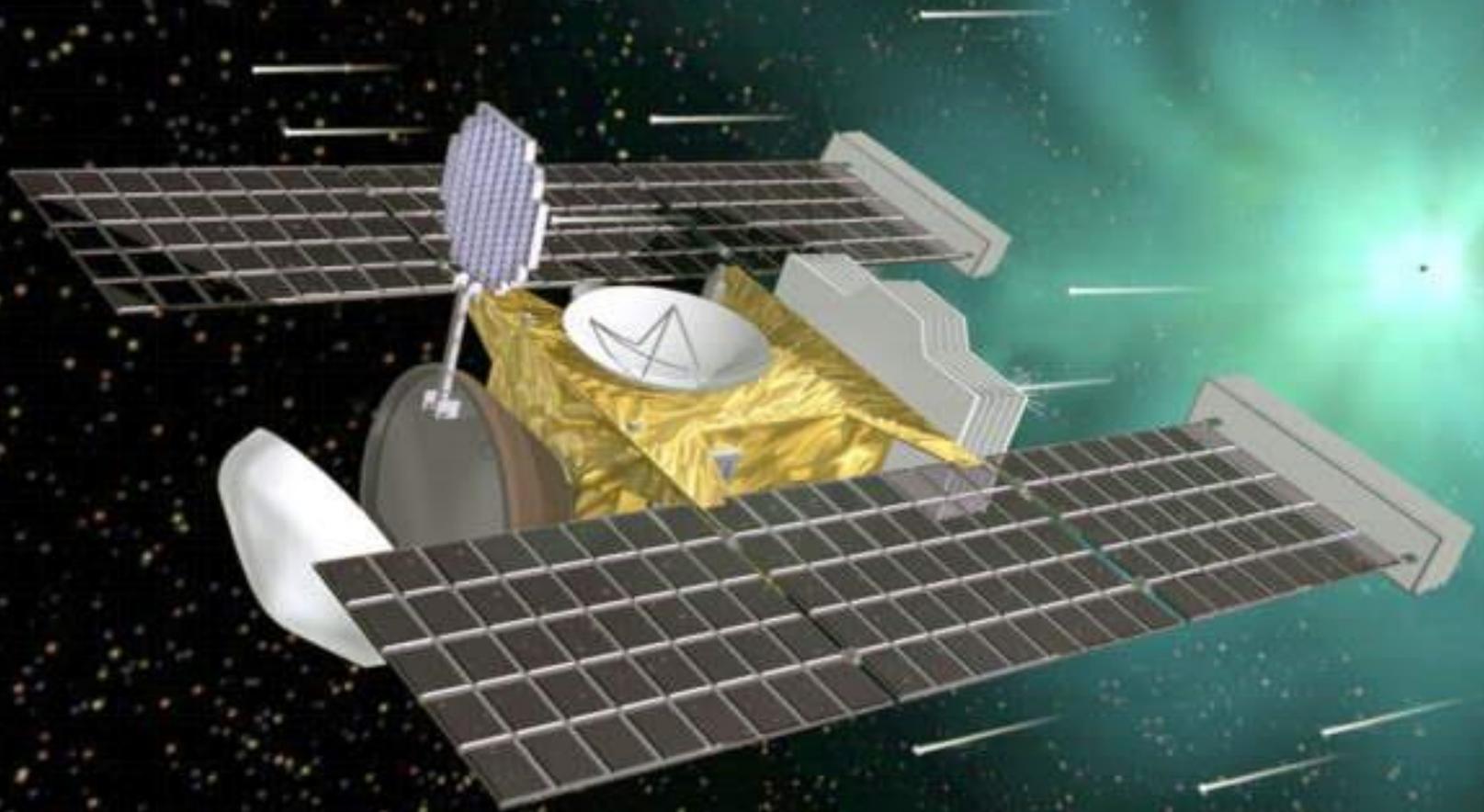
100 PetaFLOPs, 1 Exabyte (10^{18}) storage

Recently ported to Cell Phones (android) (8 billion)

Thinking@Home

Stardust@home...

Stardust (NASA)



Citizen Science Projects

- SETI@home and Astropulse (UC Berkeley)
- Stardust@home (UC Berkeley)
- SetiQuest (Seti Institute)
- Galaxy Zoo (Galaxy Classification)
- Audubon Society's Christmas Bird Count (1900)
- Community Collaborative Rain, Hail & Snow Monitor Network
- Clickworkers (mars crater identification - NASA)
- Ebird, NestWatch, FeederWatch, Urban Birds (Cornell Univ.)
- ParkScan (monitor San Francisco Parks)
- ScienceForCitizens.net
- **ENERGY@home**

Type 2 Signal Processing

Real Time in-situ Processing

Petabits per second (can not record data)

CASPER

Collaboration for Radio Astronomy
Signal Processing and Electronics Research

Some of the CASPER Collaborators:

Xilinx, Fujitsu, HP, Sun/Oracle, Nvidia, NSF, NASA, NRAO, NAIC,
CFA (Harvard/Smithsonian), Haystack (MIT), Caltech, Cornell, CSIRO/ATNF,
JPL/DSN, South Africa KAT, Manchester/Jodrell Bank, GMRT (India),
Oxford, Bologna, Metsahovi Observatory/Helsinki University,
University of California, Berkeley; Swinburne University (Australia),
Seti Institute, University of California, Santa Barbara;
University of California, Los Angeles; CNRS (France), University of Maryland
Nancay Observatory, University of Cape Town (South Africa),
ASTRON (Netherlands), Academia Sinica (Taiwan), Cambridge,
Brigham Young University, Rhodes University (South Africa)



Greenland

Iceland

Suomi
Finland

Sverige
Sweden

Norge
Norway

United Kingdom

Polska
Poland

Belgien
Belgium

Frankrijk
France

Italia
Italy

España
Spain

Ukraina
Ukraine

Türkiye
Turkey

Kazakhstan

Mongolia

中国
China

대한민국
S Korea

日本
Japan

Canada

United States

North Atlantic Ocean

México

Mauritania

Algeria

Libya

مصر
Egypt

Saudi Arabia

Iran

Afghanistan

Pakistan

ประเทศไทย
Thailand

India

Indonesia

Papua New Guinea

South Pacific Ocean

Venezuela
Colombia

Brasil
Brazil

Peru

Bolivia

Chile

Argentina

South Atlantic Ocean

Angola

Namibia

Botswana

South Africa

Kenya

Tanzania

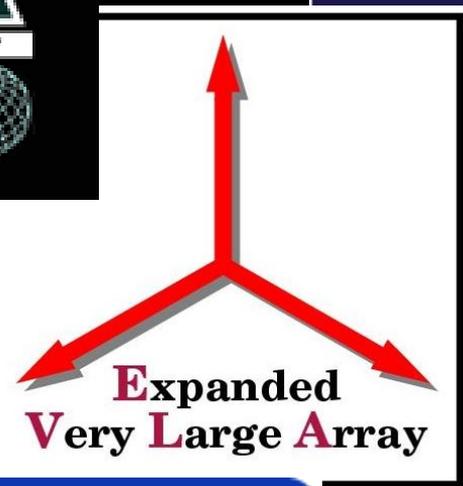
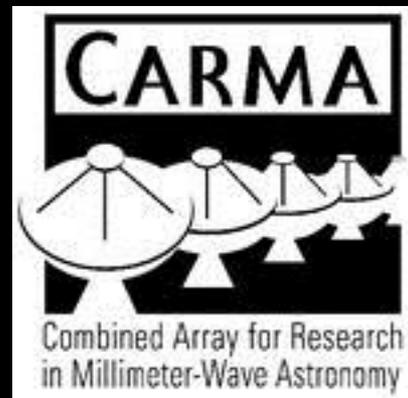
Madagascar

Indian Ocean

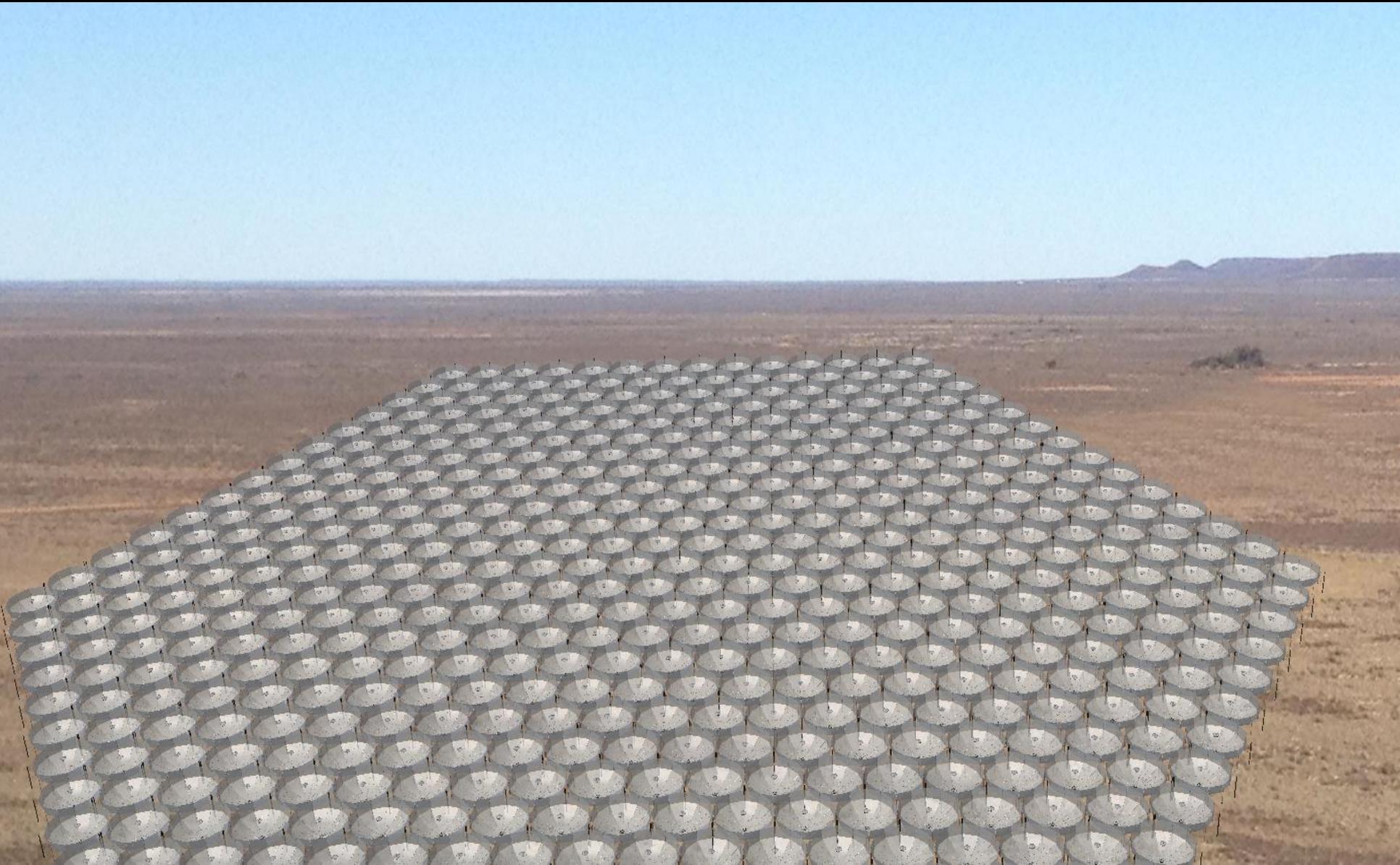
Australia

New Zealand

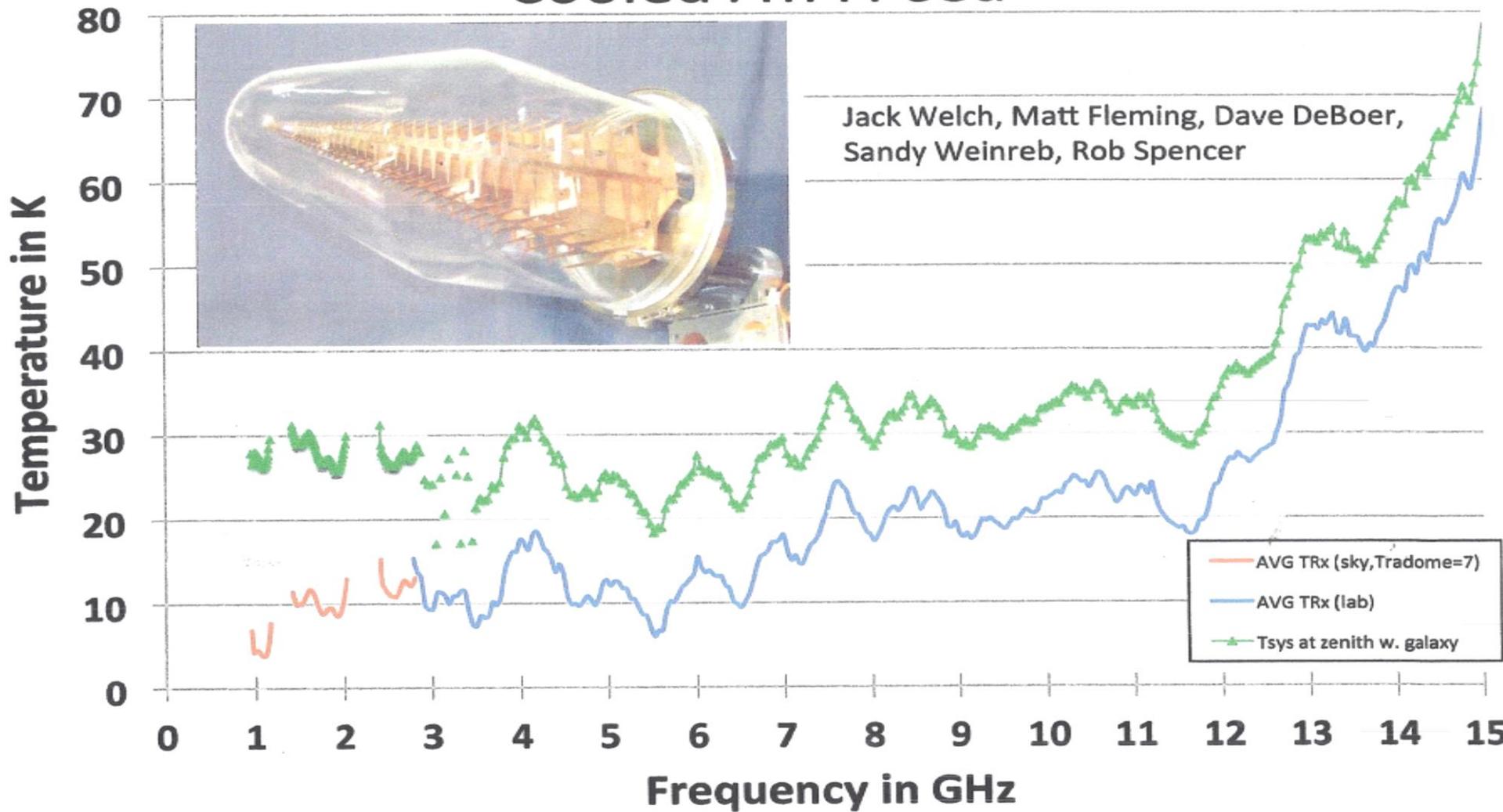
MWA
XNTD
PAPER
FAST
PAST
LAR
LWA



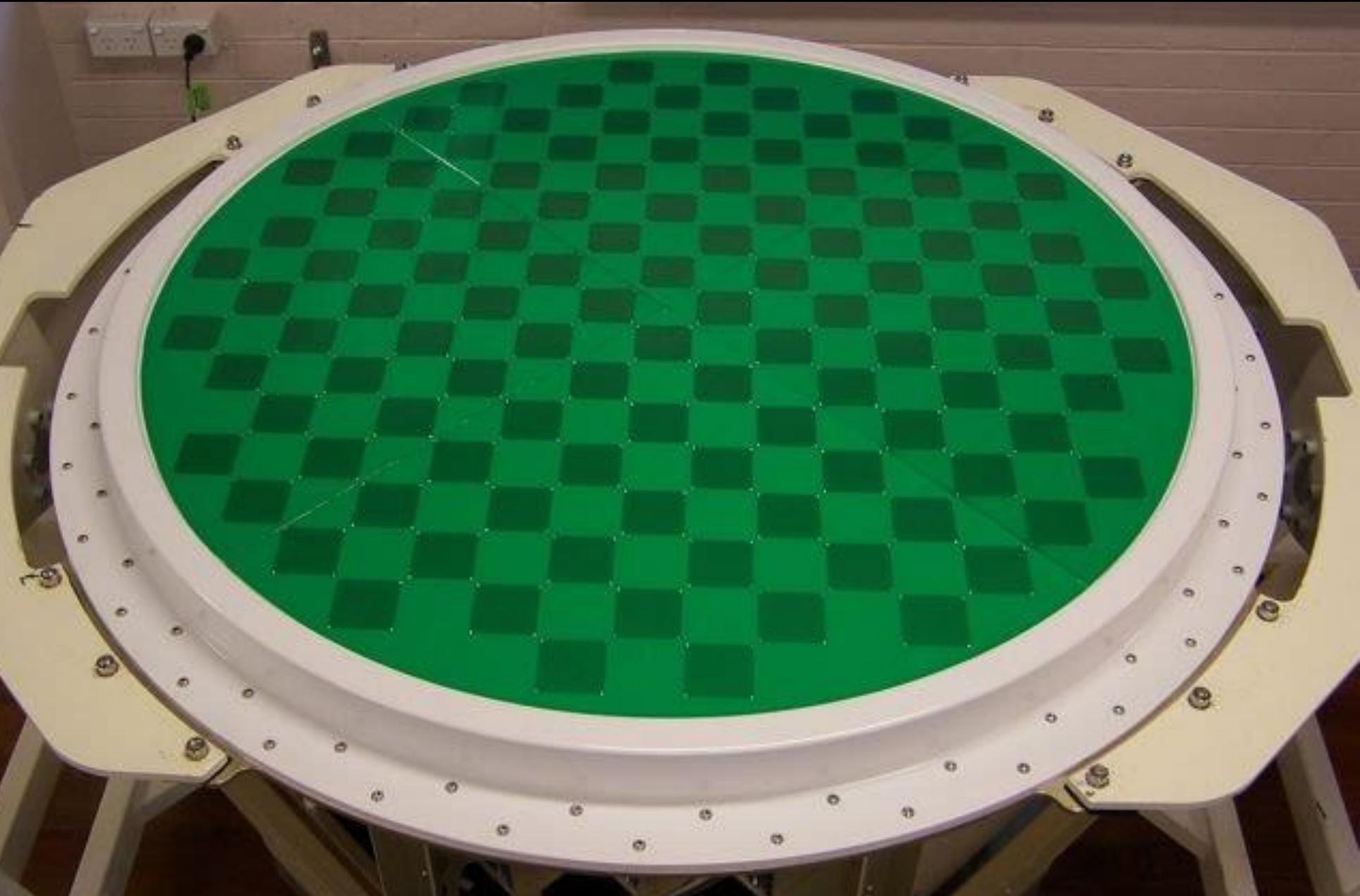
HERA Array 547 x 15 meter dishes

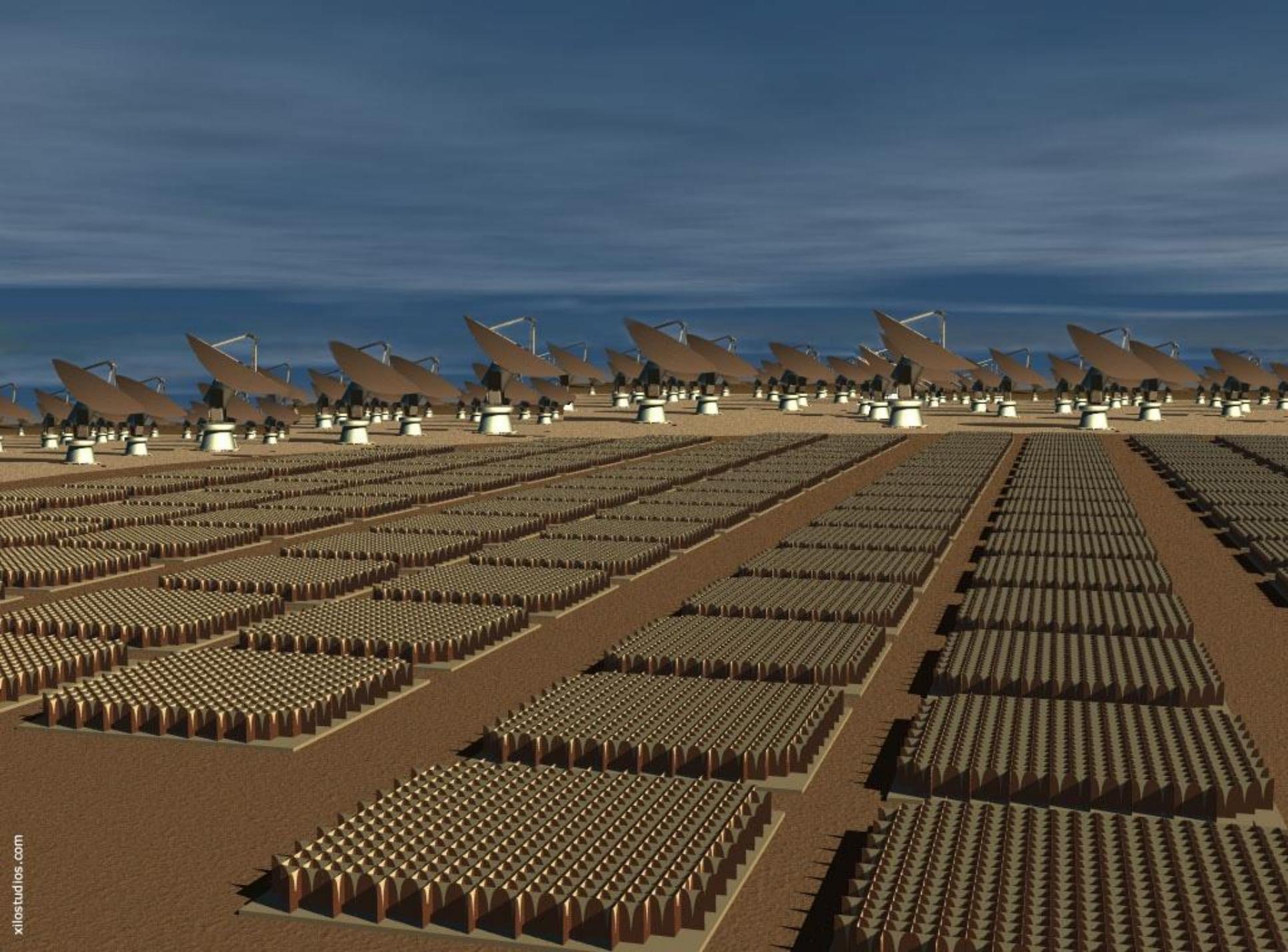


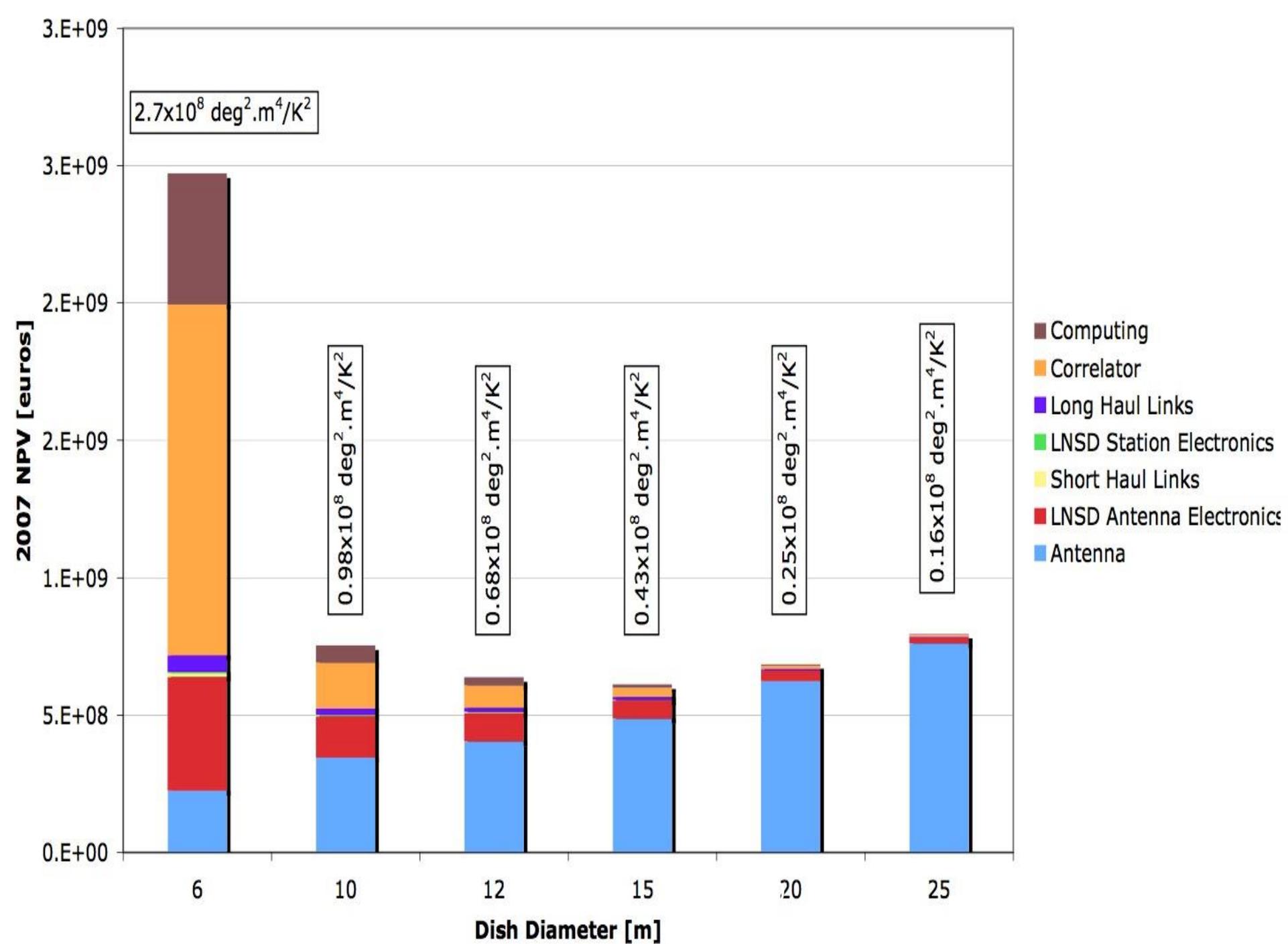
Measured Receiver Temperature & T_{sys} at Zenith Cooled ATA Feed



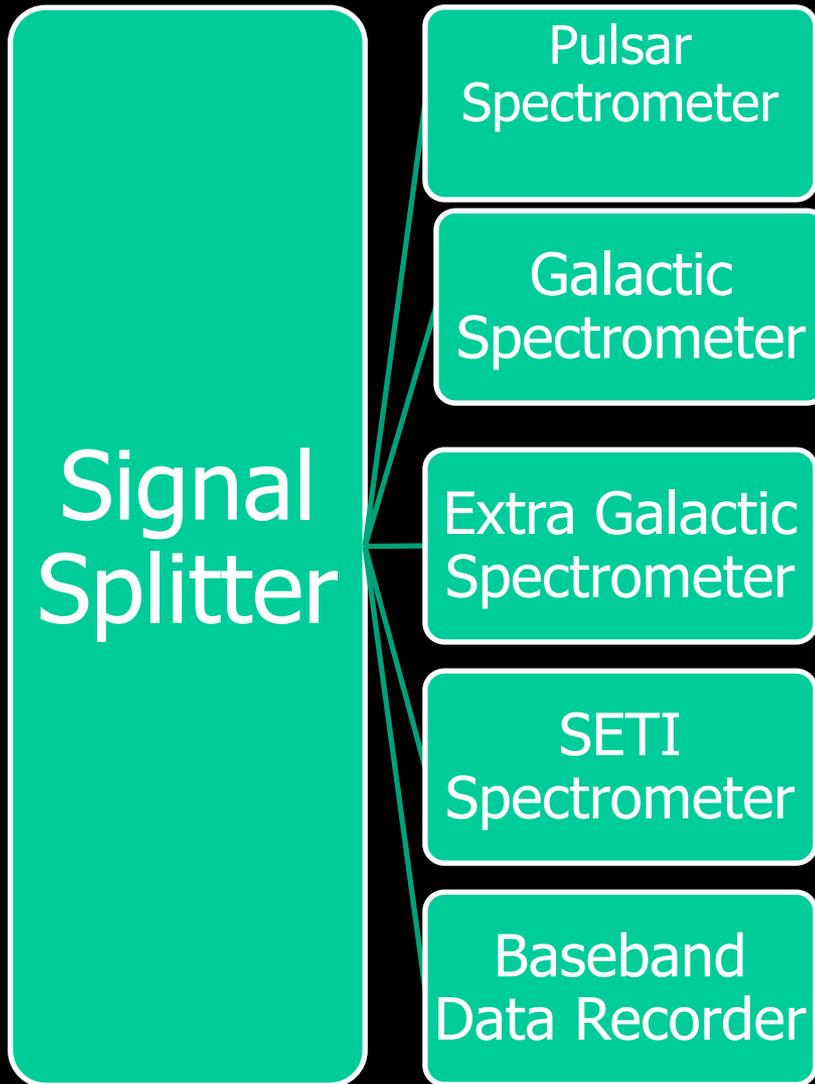
Phased Array Feed – 64 beams







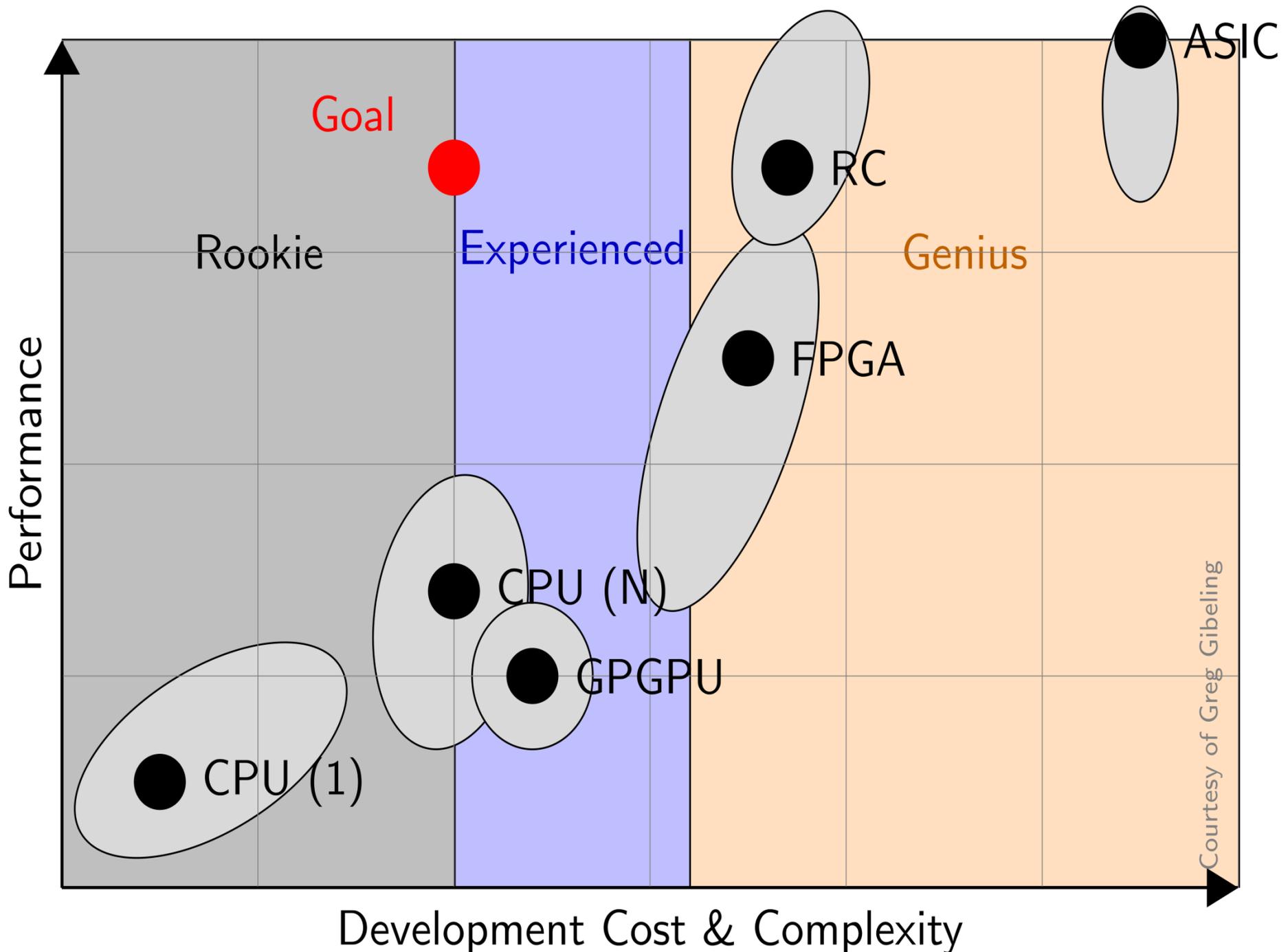
Simultaneous Digital Backends Piggyback, Commensal, Sky Surveys



Analog Power Splitters

or

Digital Data Splitter



Courtesy of Greg Gibeling

FPGA vs GPU

FPGA = synchronous, GPU = asynchronous

eg: ADC input: FPGA to time stamp, packetize

FPGA: 1 Tbit/sec I/O GPU: 18 Gbit/sec

GPU's use more power (3 - 20X FPGA)

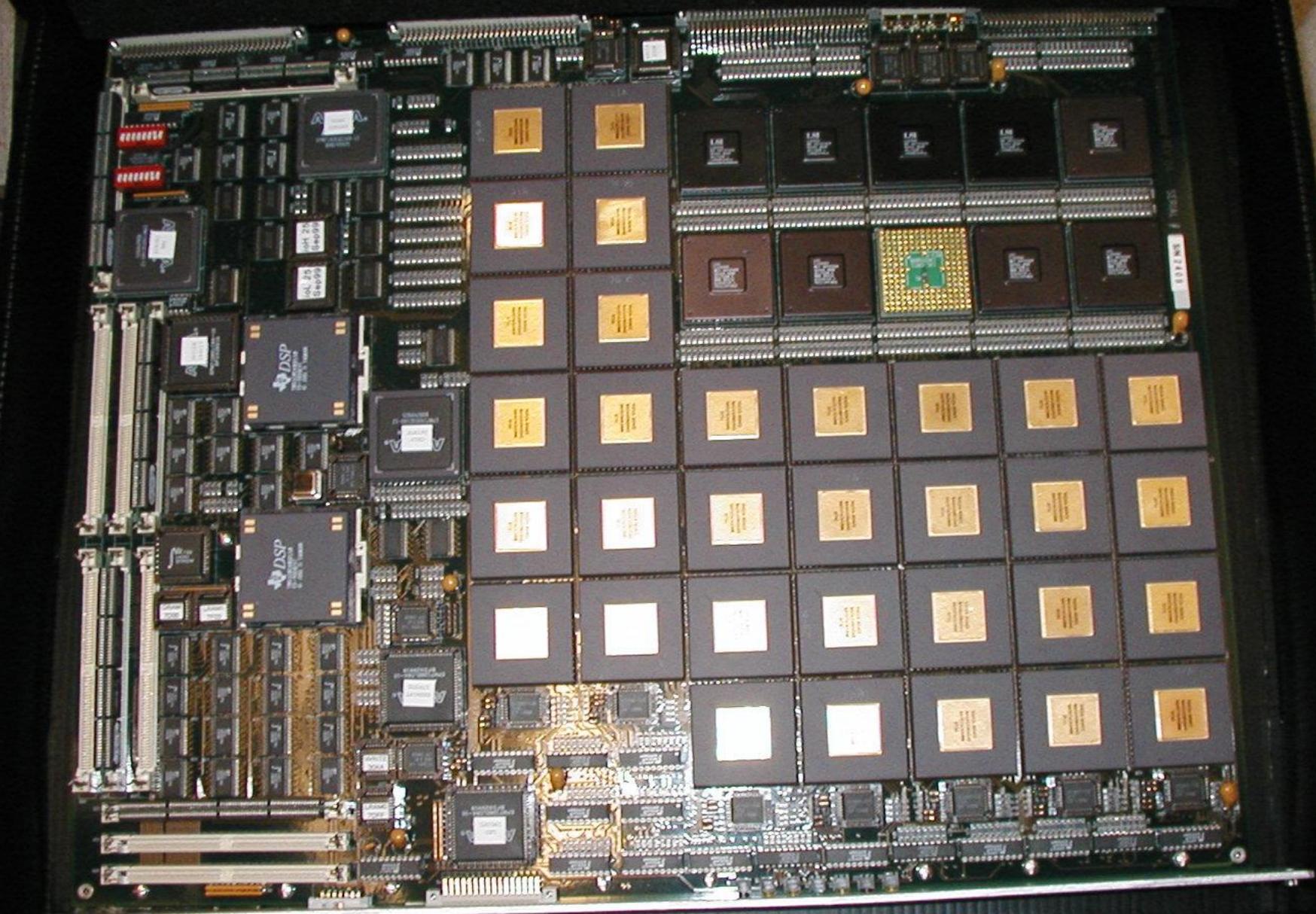
GPU's are easier to program (CUDA)

GPU's are cheaper

GPU's are good at floating point

The Problem with the Traditional Hardware Development Model

- Takes 5 to 10 years
- Cost Dominated by NRE because of custom Boards, Backplanes, Protocols
- Antiquated by the time it's released.
- How to buy the hardware at the last minute?
- Each observatory designs from scratch





Solution:

Modular General Purpose Hardware

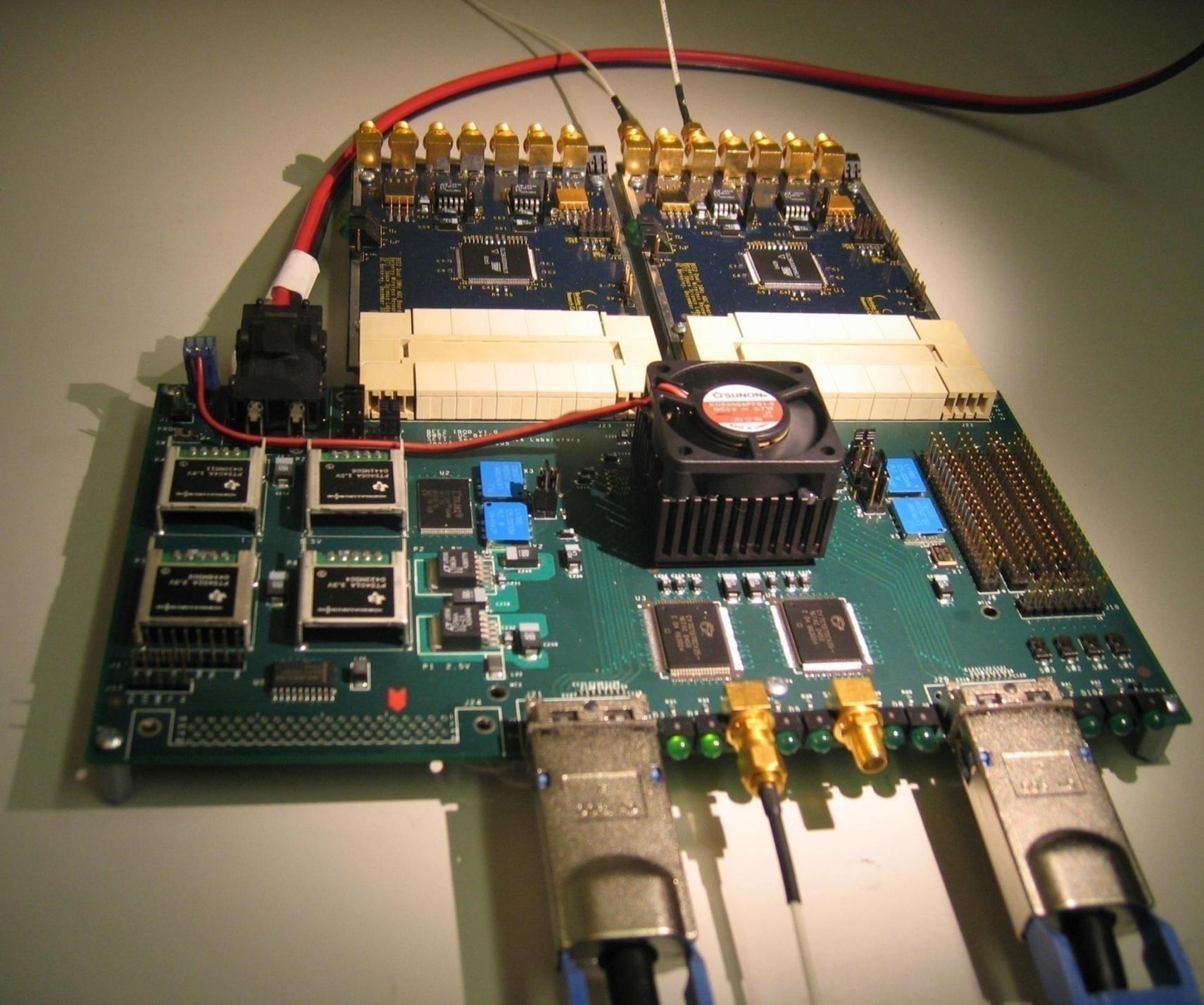
- Low number of board designs
- Can be upgraded piecemeal or all together
- Reusable
- Standard signal processing model which is consistent between upgrades.

CASPER Real-time Signal Processing Instrumentation

- Low NRE, shared by the community
- Rapid development
- Open-source, collaborative
- Reusable, platform-independent gateware
- Modular, upgradeable hardware
- Industry standard communication protocols
- Use switches to solve correlator interconnect
- Low Cost

Collaboration

- Share Open Source Libraries
- Workshops
- Video's and Doc's on Tool Flow, Libraries
- Wiki, Mailing List
- Open Source Boards (available from vendors)

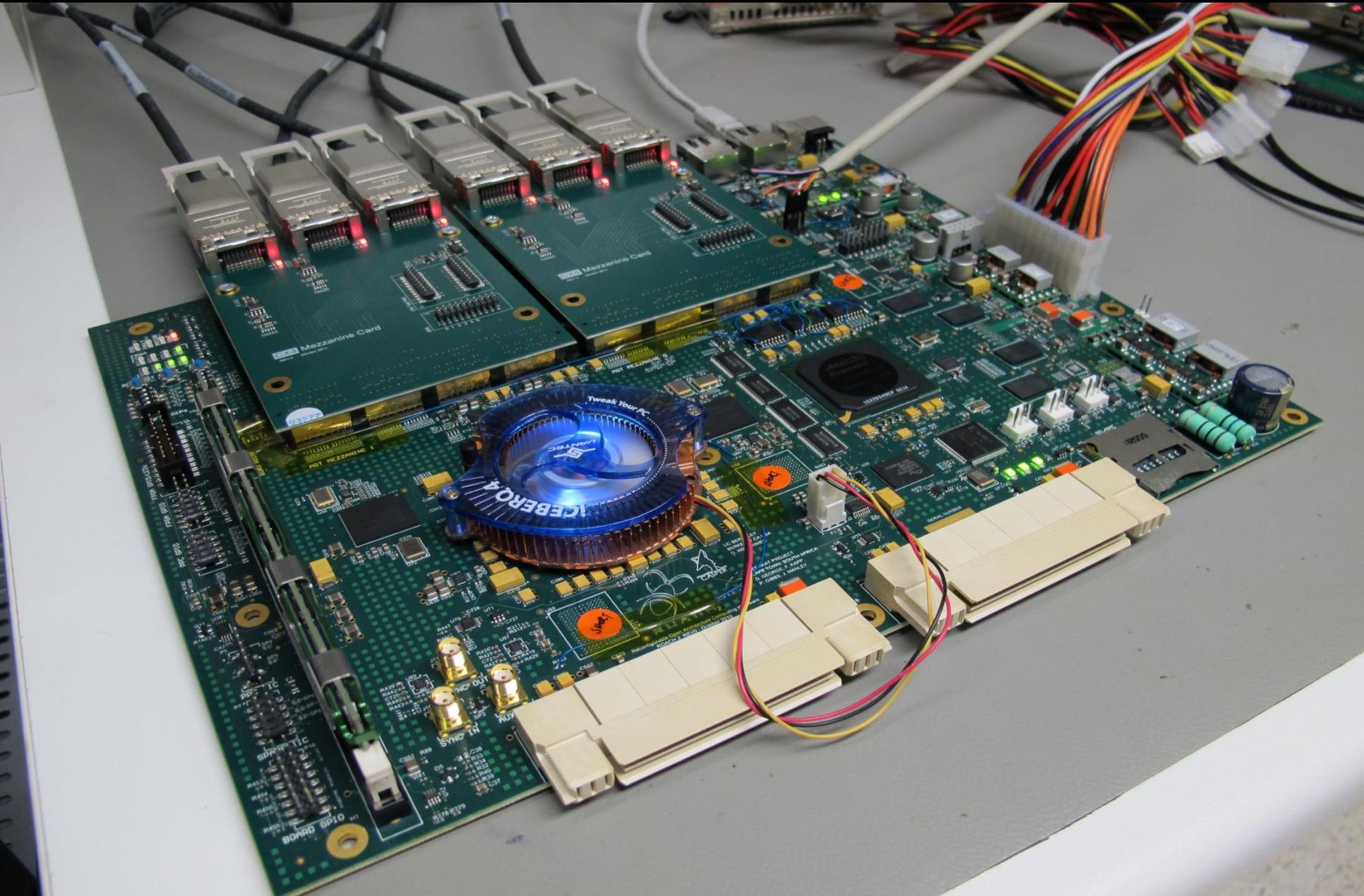




Roach Motel (Roach Nest) (KAT)



Roach II (South Africa KAT)



Current CASPER ADC Boards

ADC2x1000-8 (dual 1GSa/sec, single 2Gsps, 8 bit)

ADC1x3000-8 (3GSa/sec, 8 bit) ADC (6Gsps interleaved)

64ADCx64-12 (64x 64MSa/sec, 12 bit)

ADC4x250-8 (quad 250MSa/sec, 8 bit)

katADC (dual 1.5GSa/sec, 8 bit, with gain, atten, synth)

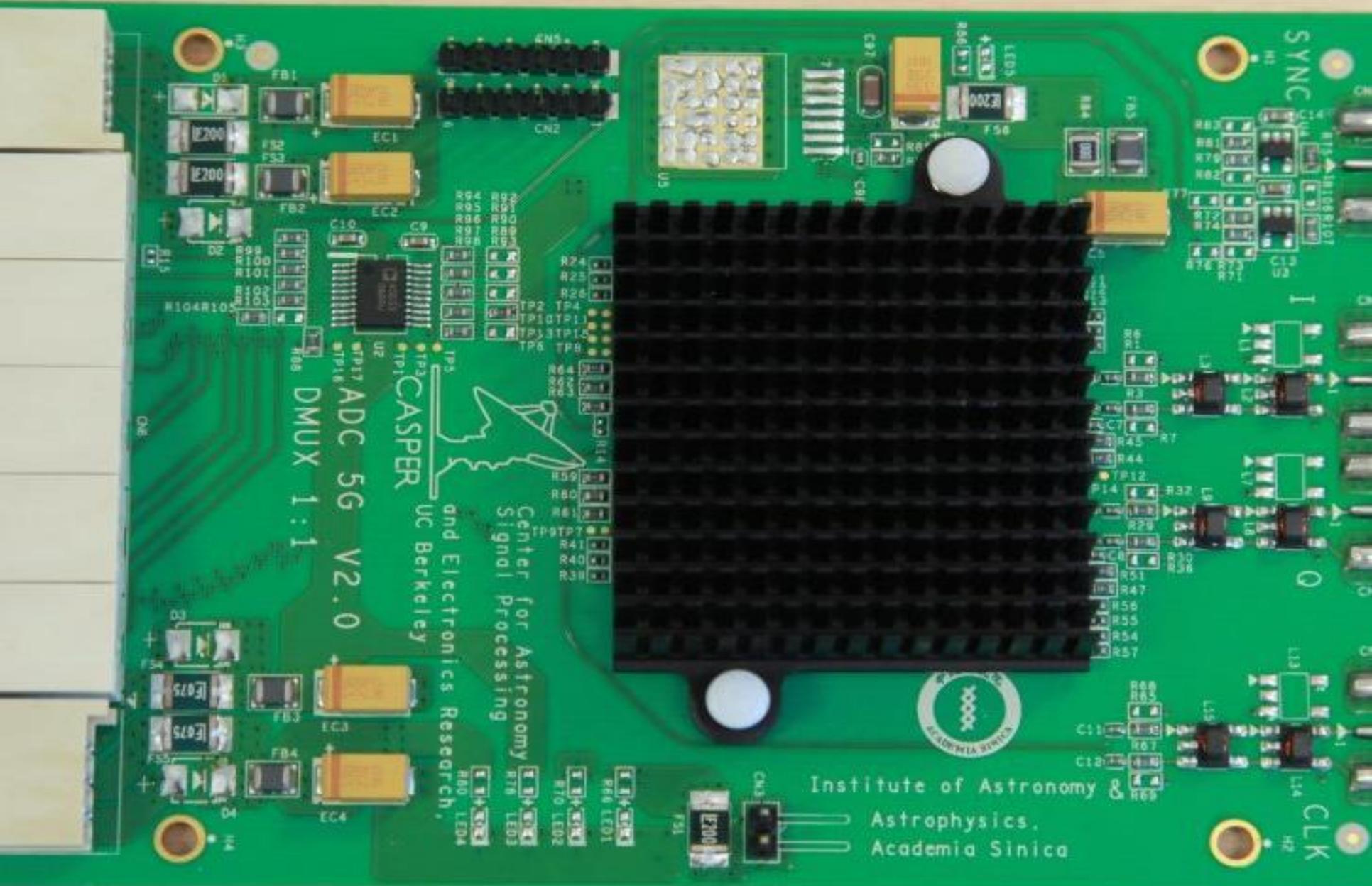
ADC2x550-12 (dual 550 Msps, 12 bit)

ADC2x400-14 (dual 400 Msps, 14 bit)

ADC1x5000-8 (1x5Gsps, 2x2.5Gsps, ASIAA - Taiwan)

ADC1x1000-12 (optically isolated 12 bit 1Gsps – JPL)

5 Gps, 8 bit ADC - ASIAA (tested at ASIAA, CFA, NRAO, UCB)



DMUX 1:1
ADC 5G V2.0

CASPER
UC Berkeley

Center for Astronomy
and Electronics Research,
Signal Processing

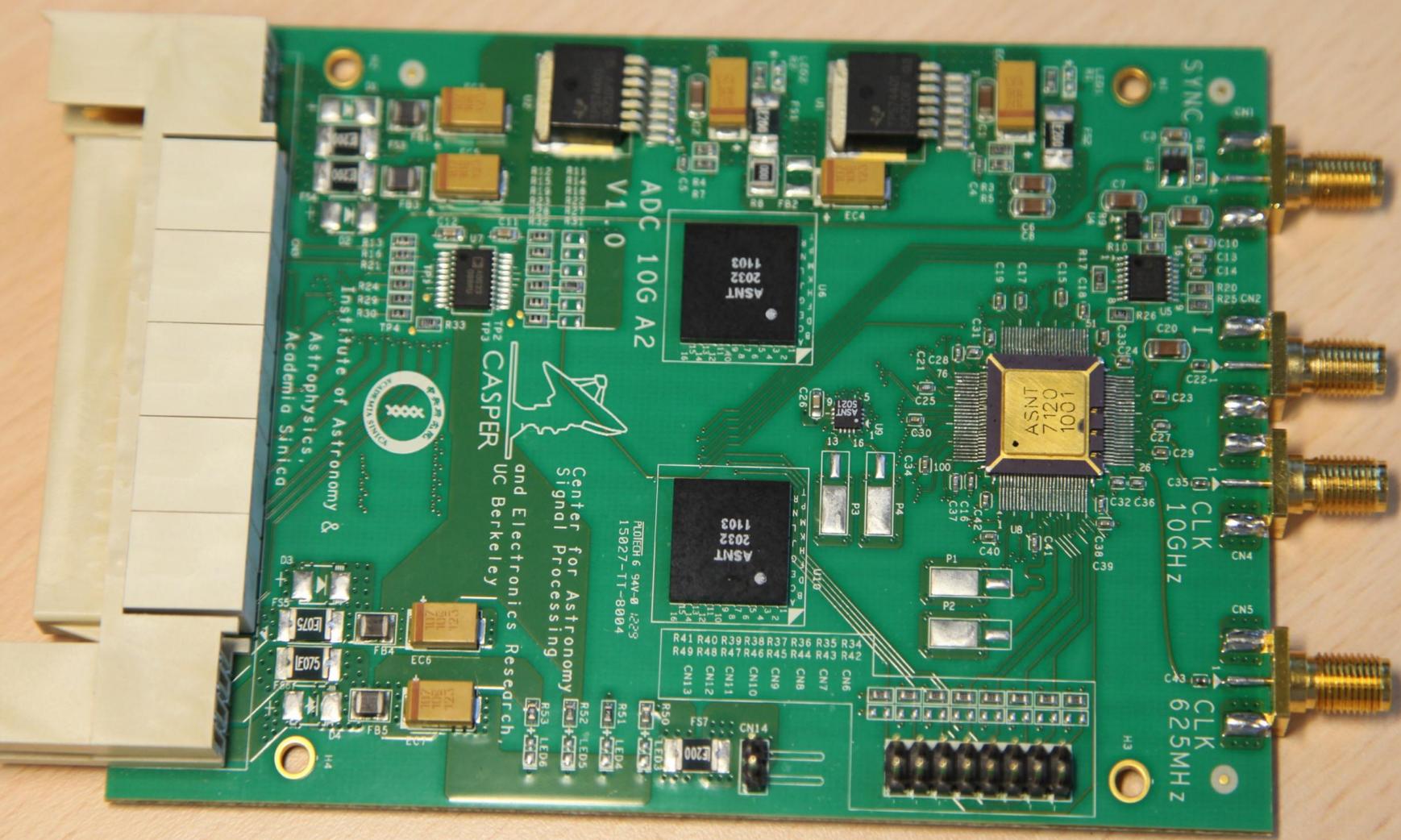


Institute of Astronomy &
Astrophysics,
Academia Sinica

SYNC

CLK

10 Gps 4 bit ADC: ASIAA Kim Guizino



20 to 60 Gsps ADC's ??

26 Gsps	3.5 bit	Hittite ADC
20 Gsps	5 bit	E2V ADC
60 Gsps	8 bit	Fujitsu
20 Gsps	6 bit	Micram

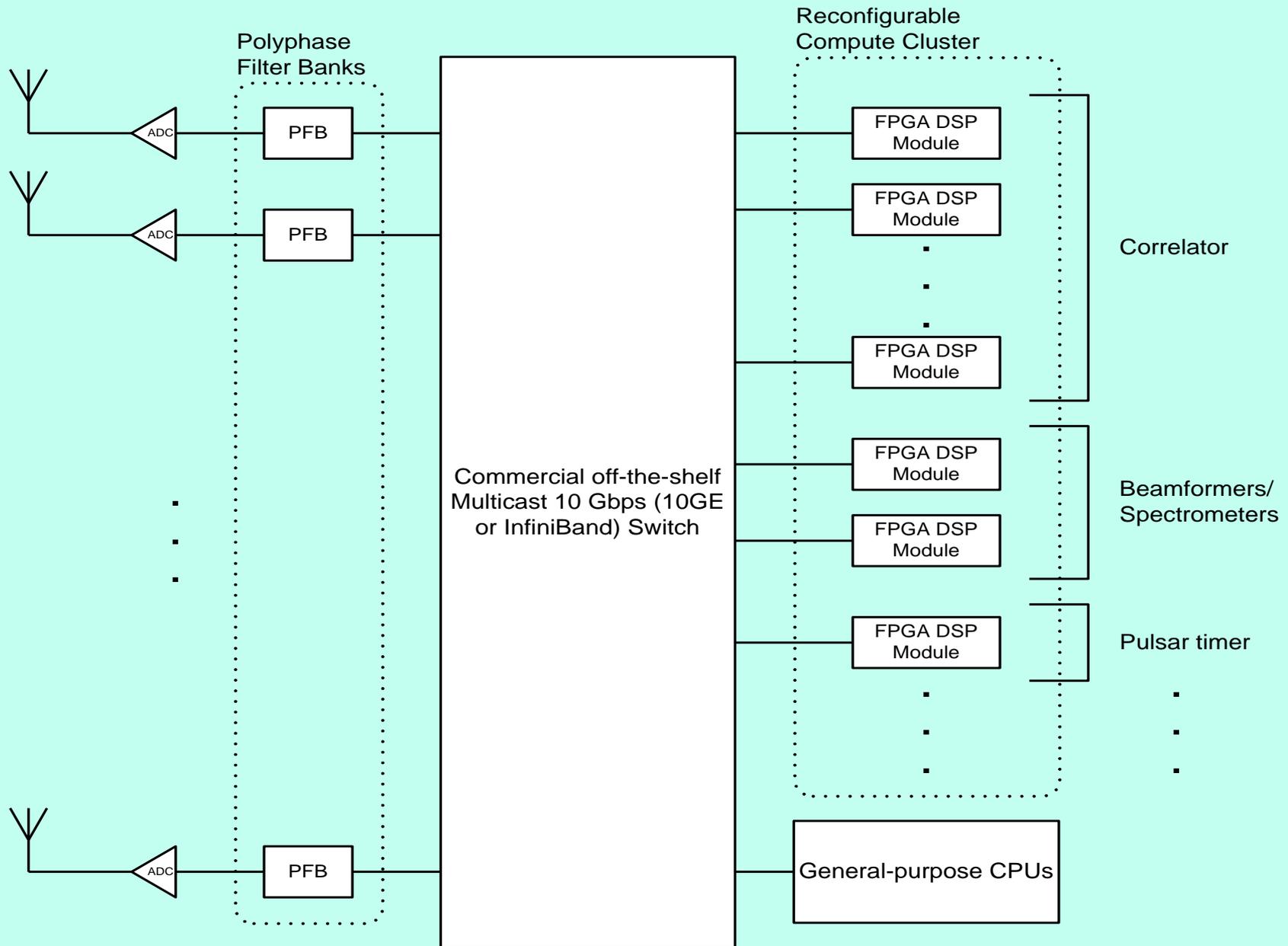
Board Interconnect - Upgradable

- Problem: Backplanes are short lived
(S100, Multibus, VME, ISA, EISA, PCI, PCIx, PCIE, PCIE2.0, compactPCI, compactPCIE, ATCA...)
- Solution: Use 10Gbit Ethernet (40/100 Gbe)
(10Gbe, Infiniband, Myrinet, Xaui, Aurora)
Copper CX4/SFP+ (15 meters max) or Optical



Beowulf Cluster Like General Purpose Architecture

Dynamic Allocation of Resources, need not be FPGA based



Serendip VI & ALFABURST (Hemant Shukla, NSF) UCB, WVU, Oxford, Arecibo (and soon, GBT)



10, 40 Gbit Ethernet Switches, NIC's

Fujitsu, Arista Cisco, Force10, Fulcrum, Extreme Networks, HP, Mellanox... (\$85 per port)

CX4 connectors (old), RJ45, SFP+ (standard)

756 10Gbe ports or 300 40Gbe ports
full crossbar, non blocking - available now
(big enough for SKA already, 20 Tbit/sec)

40 and 100 Gbit ethernet switches available now

inexpensive 1U switch: 36x40Gbe or 144x10Gbe

Platform-Independent, Parameterized Gateway

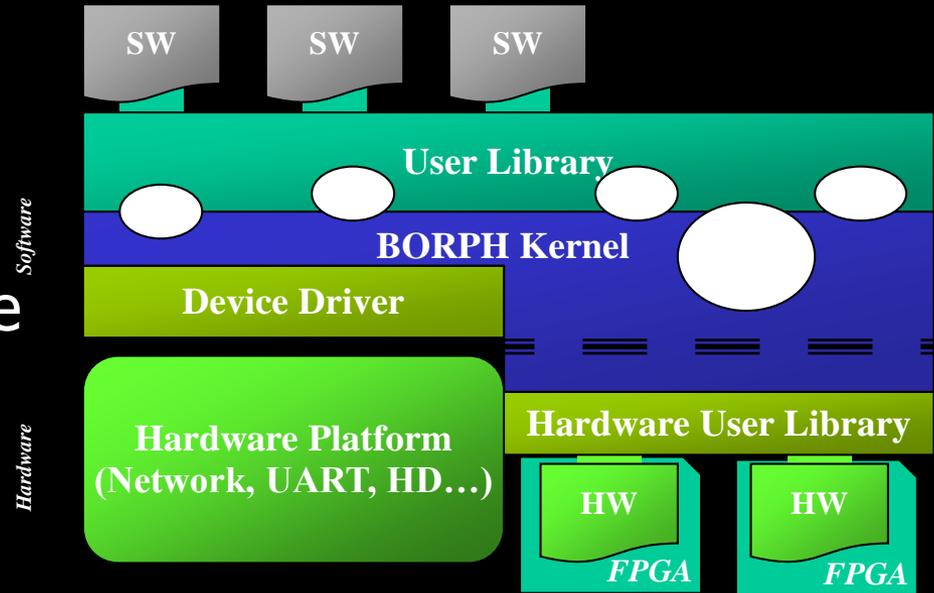
- Libraries for signal processing which don't have to be rewritten every hardware generation.
- Matlab Simulink
- Linux File I/O and Process Control

Borph – Hayden So

FPGA device Drivers – Shanly Rajan

BORPH Operating System – Hayden So and fast FPGA device drivers – Shanly Rajan

- An extended version of Linux operating system
 - Treats FPGAs = CPUs
- FPGA applications execute as hardware processes
- HW/SW communication
 - UNIX file I/O
- Benefits
 - Easy to understand for novice/experienced users
 - **Remote control+monitor**

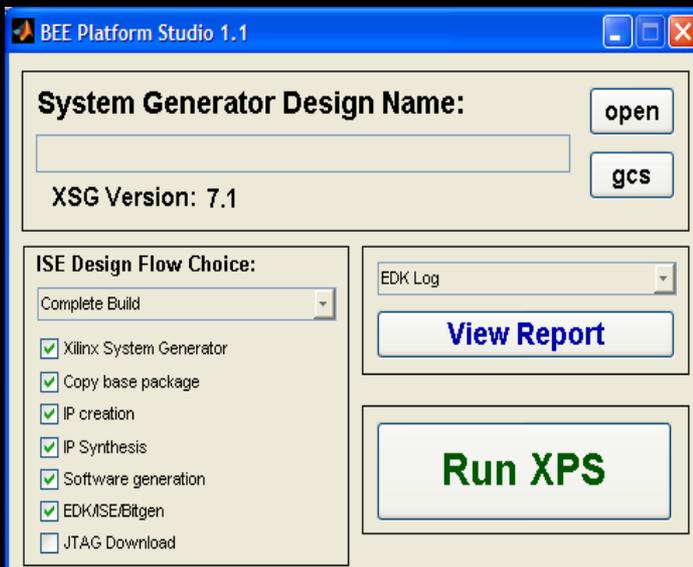
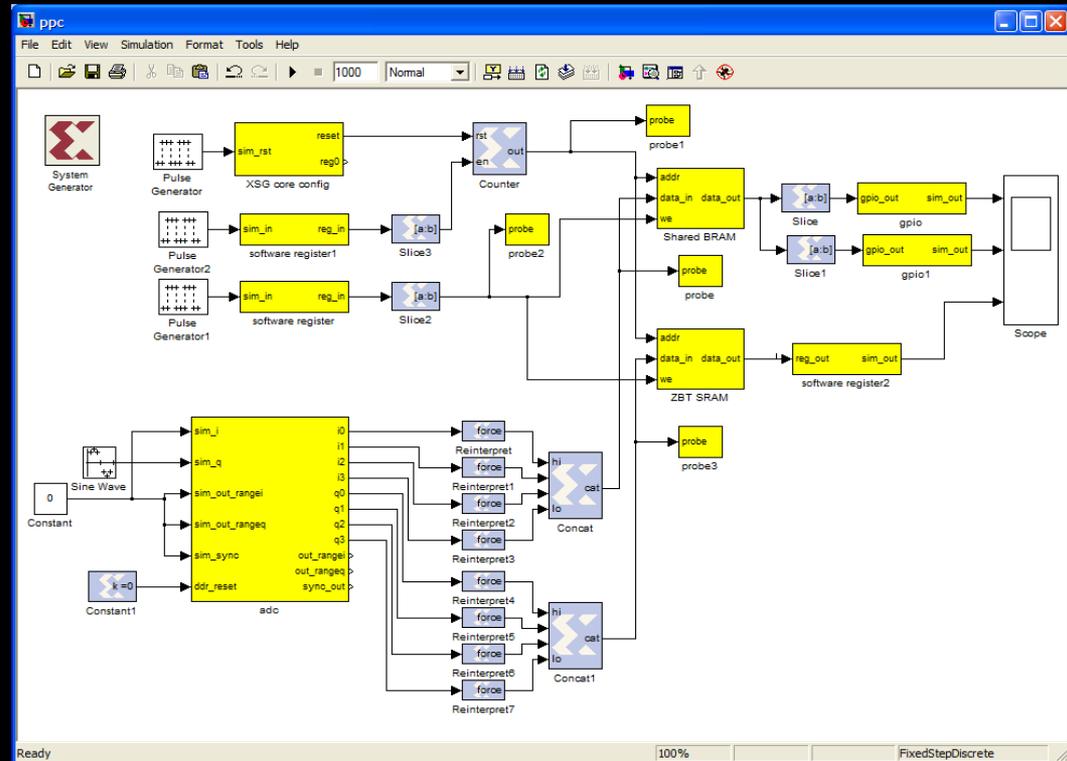
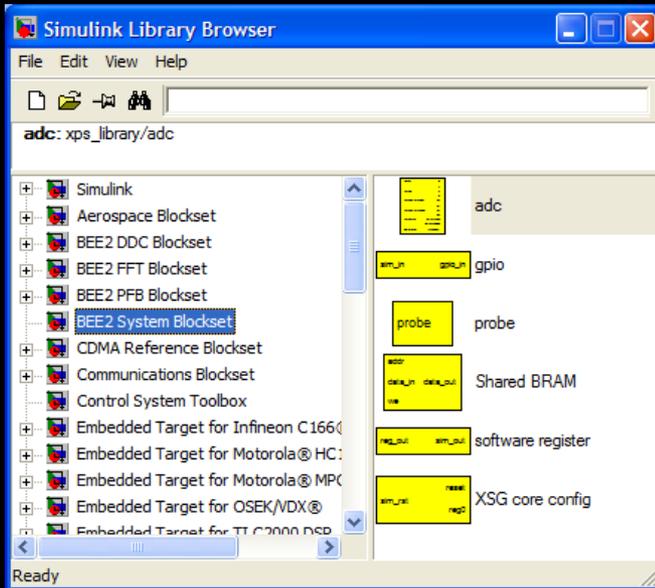


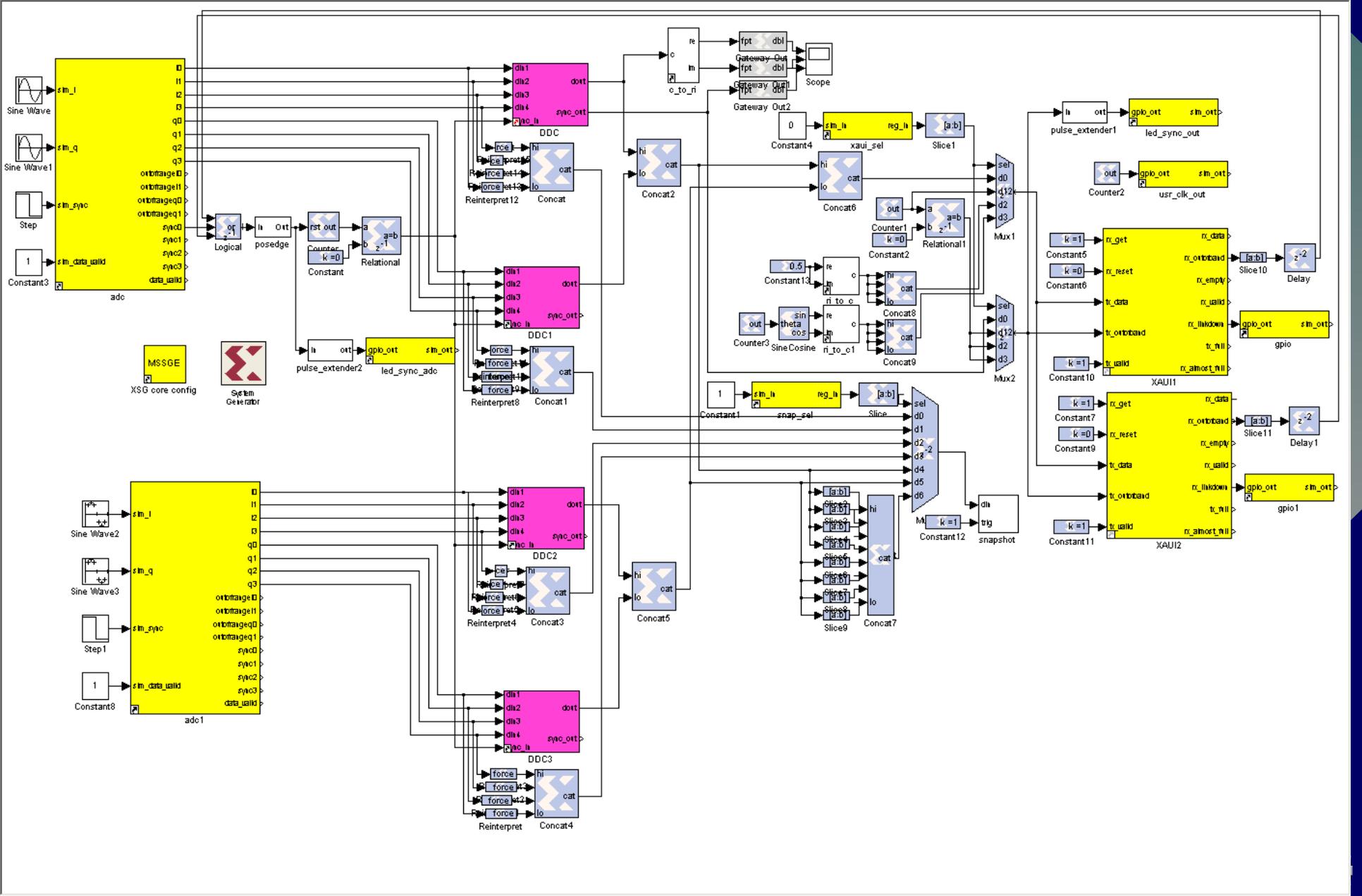
Poster Session 3 P3_09

(11am):

File System Access From
Reconfigurable FPGA
Hardware Processes in
BORPH

Simulink-based Design Tool Flow



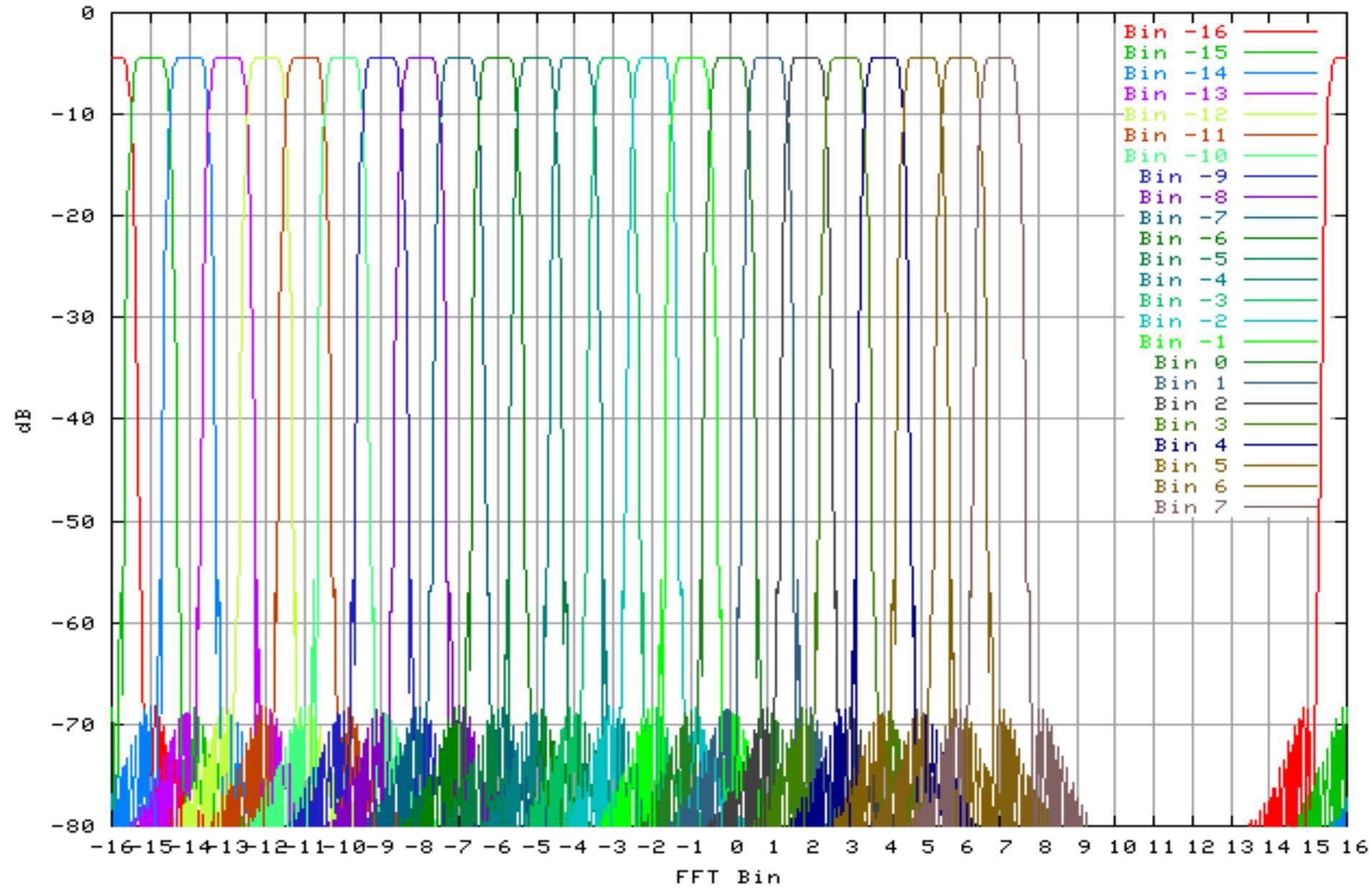


FFT controls

Simulink Library

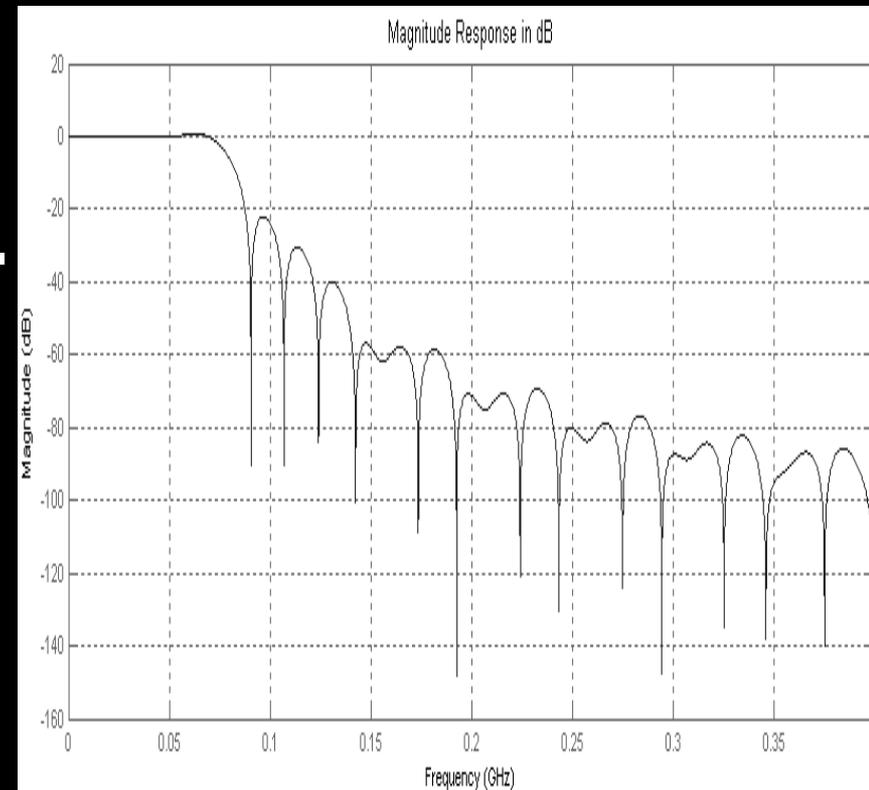
- Transform length
- Bandwidth
- Complex or Real
- Number of Polarizations
- Input bit width and output bit width
- twiddle coefficient bit width
- Run-time programmable down-shifting
- Decimate option

PFB vs. FFT

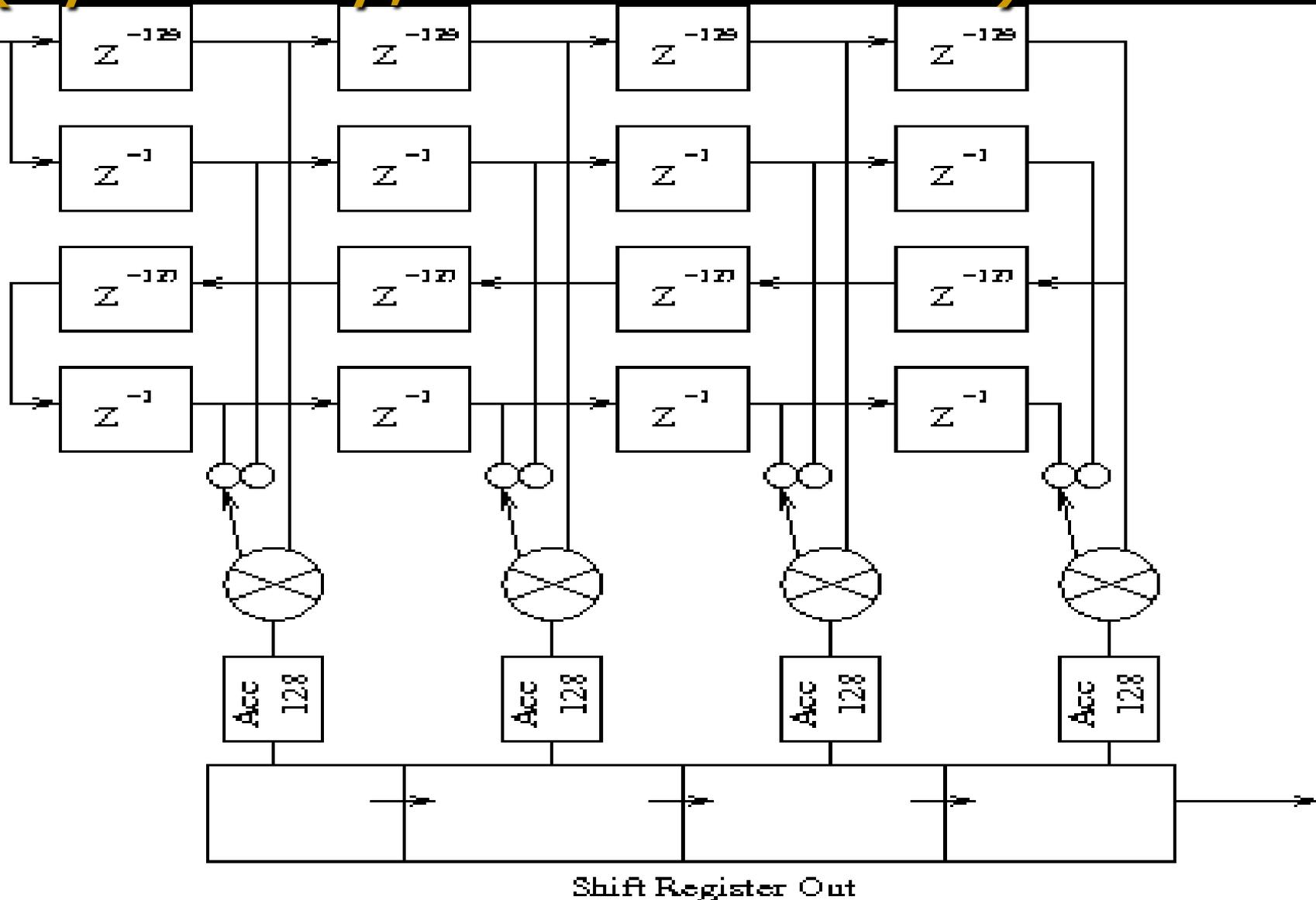


Digital Down-Converter

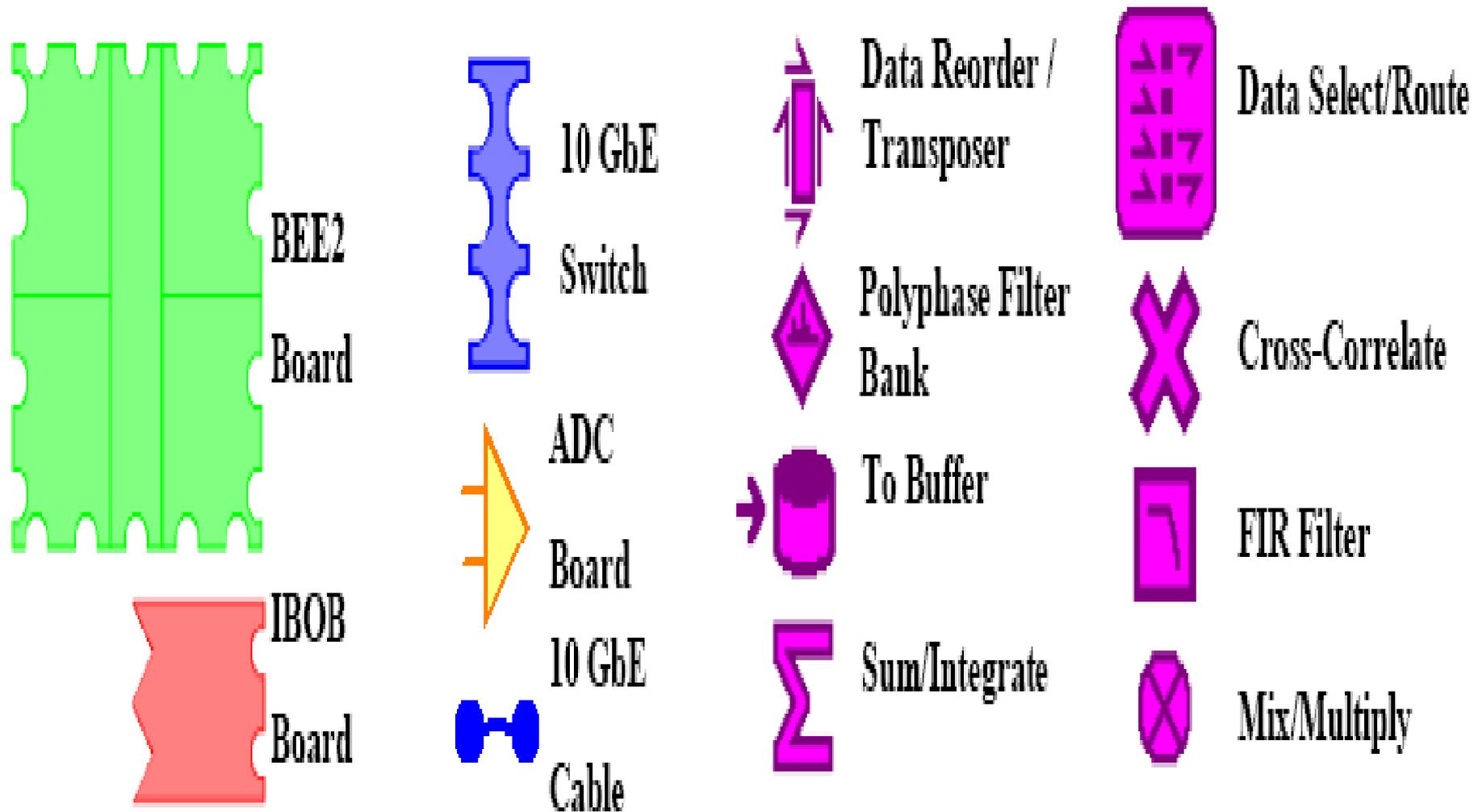
- Selectable # of FIR taps
- On-the-fly programmable mix frequency
- Selectable FIR coeff
- Agile sub-band selection.



X-Engine Correlation Architecture (Lynn Urry, Aaron Parsons)

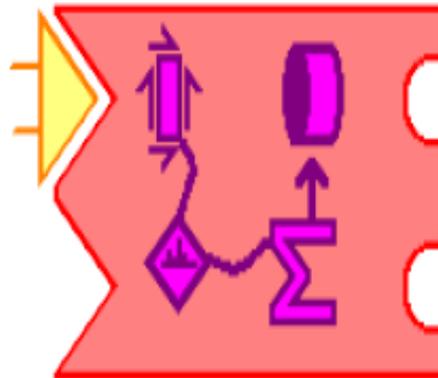


Hardware and Software Libraries legend:

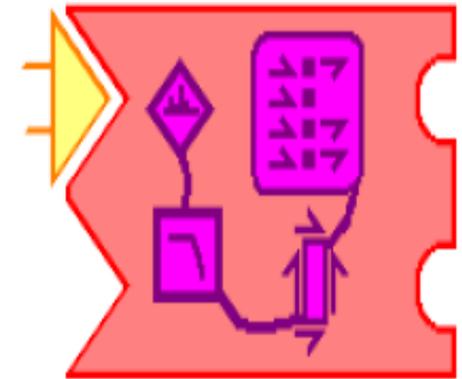


Applications

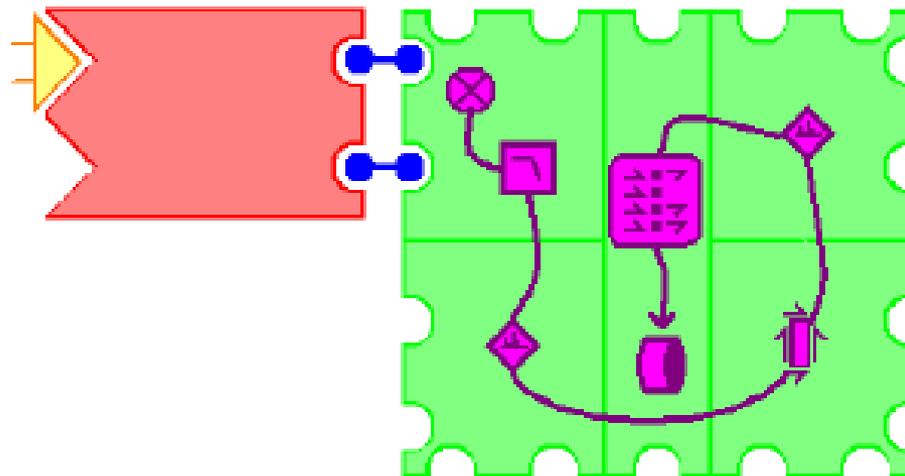
1) Pocket Spectrometer:



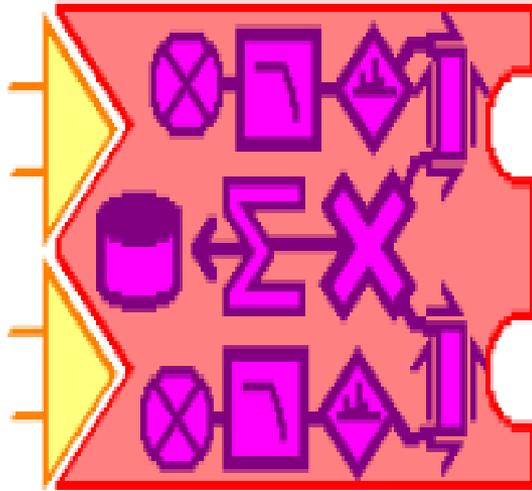
2) VLBI Channelizer:



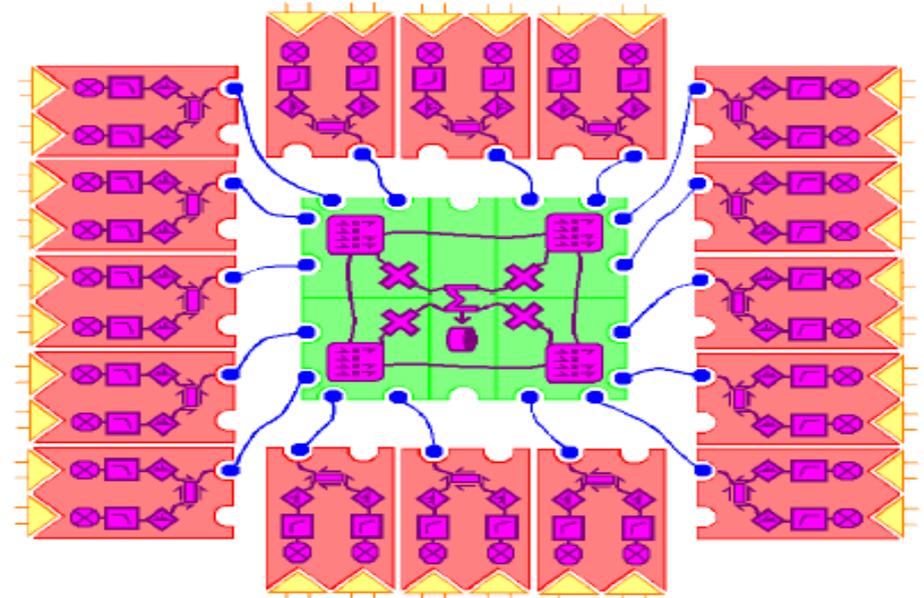
3) SETI Spectrometer:



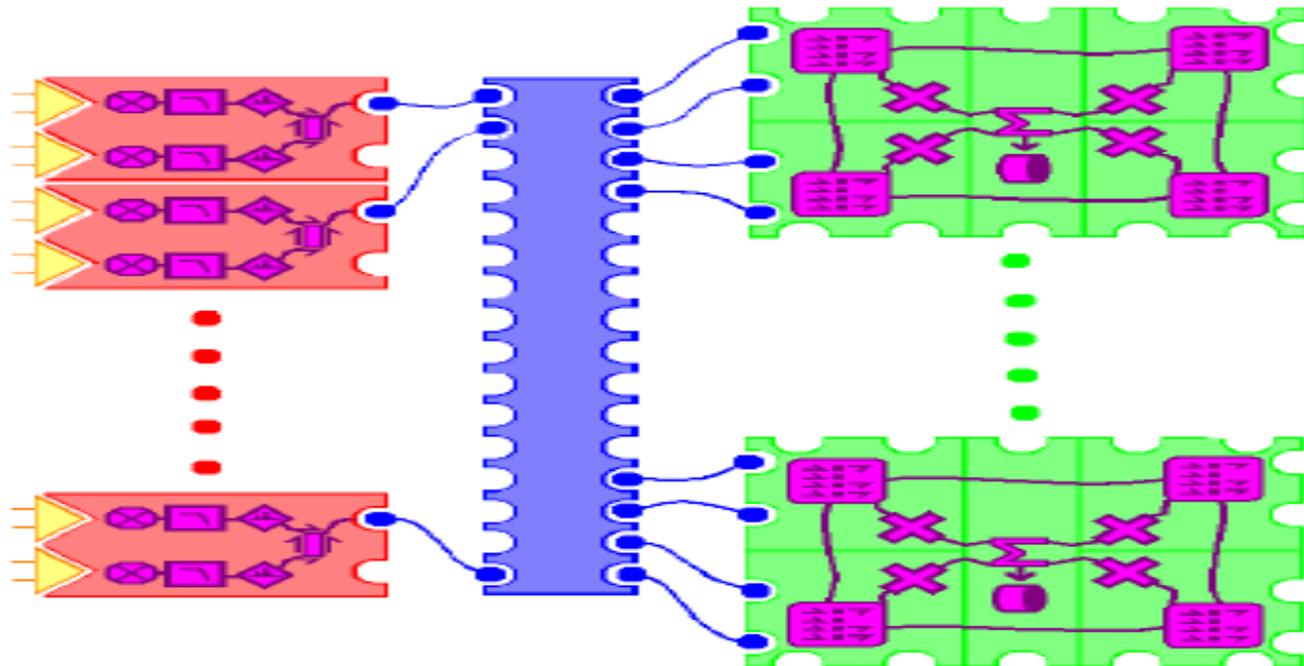
4) Pocket Correlator:



5) 32 Station Correlator:



6) Arbitrary Sized Correlator



Applications

- VLBI /VLBA/eVLBI Mark 5: Haystack, NRAO, CARMA, SMA, Finland...
- Beamforming – ATA, SMA, CARMA, SKADS, MIT
- SETI – Arecibo (UCB), DSN (JPL/UCB), GBT (NRAO/UCB)
- Correlators and Imagers:
 - ATA, Oxford (SKADS), MIT (FFT imaging correlator)
 - PAPER (Reionization Experiment)
 - Carma Next Gen,
 - MeerKAT/SKA South Africa
 - GMRT next gen correlator ??
 - Bologna (SKA), FASR ??
- Pulsar Timing and Searching, Transient
 - Green Bank, Arecibo, Allen Telescope Array, VLA,
 - Swinburne (Parkes), meerKAT, Nancay, Effelsburg

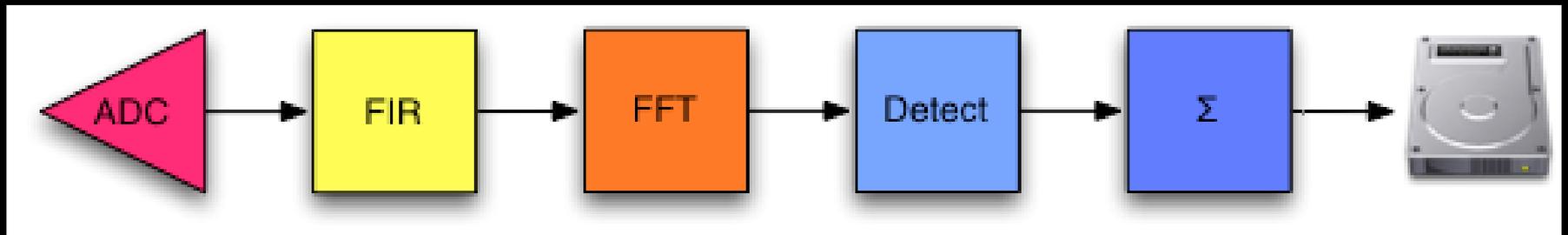
SETI Spectrometers

- Parkes Southern SERENDIP
- ALFA SETI Sky Survey (300 MHz x 7 beams)
- JPL DSN Sky Survey (eventually 20 GHz bandwidth)

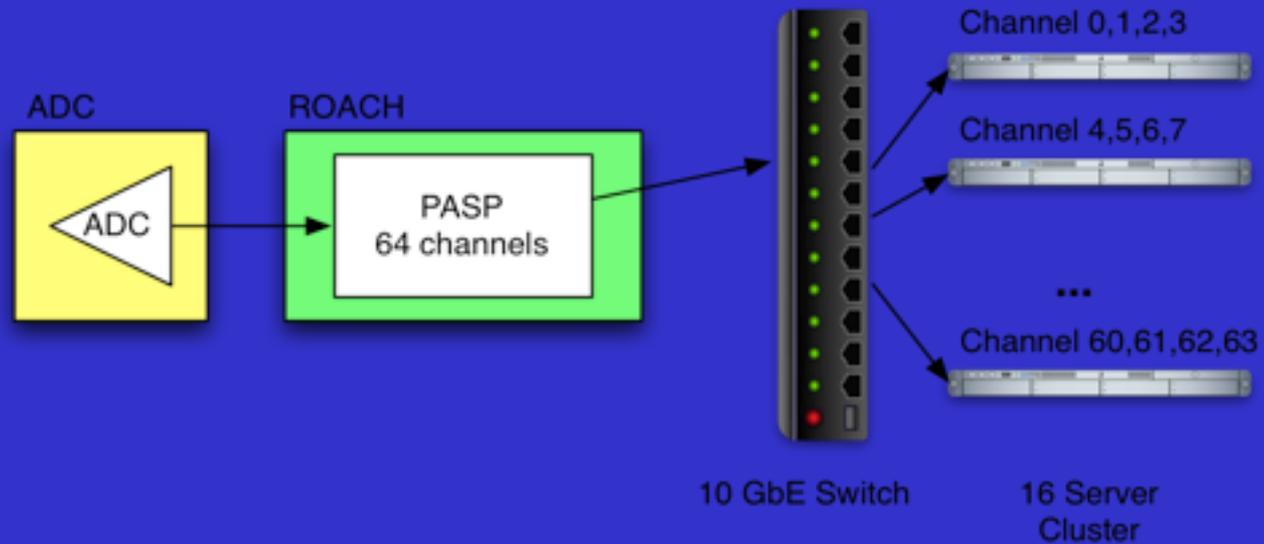
Radio Astronomy Spectrometers

- GALFA Spectrometer – Arecibo Multibeam Hydrogen Survey
- Astronomy Signal Processor – ASP – Don Backer, Ingrid Stairs, et al(pulsars)
- Antenna Holography, ATNF, China
- Gavert (DSN education, outreach) – 8 GHz BW –G. Jones
- CMB Bolometer Readout – Caltech, UCB
- Fast Readout Spectrometers (Parkes, NRAO, ATA...)

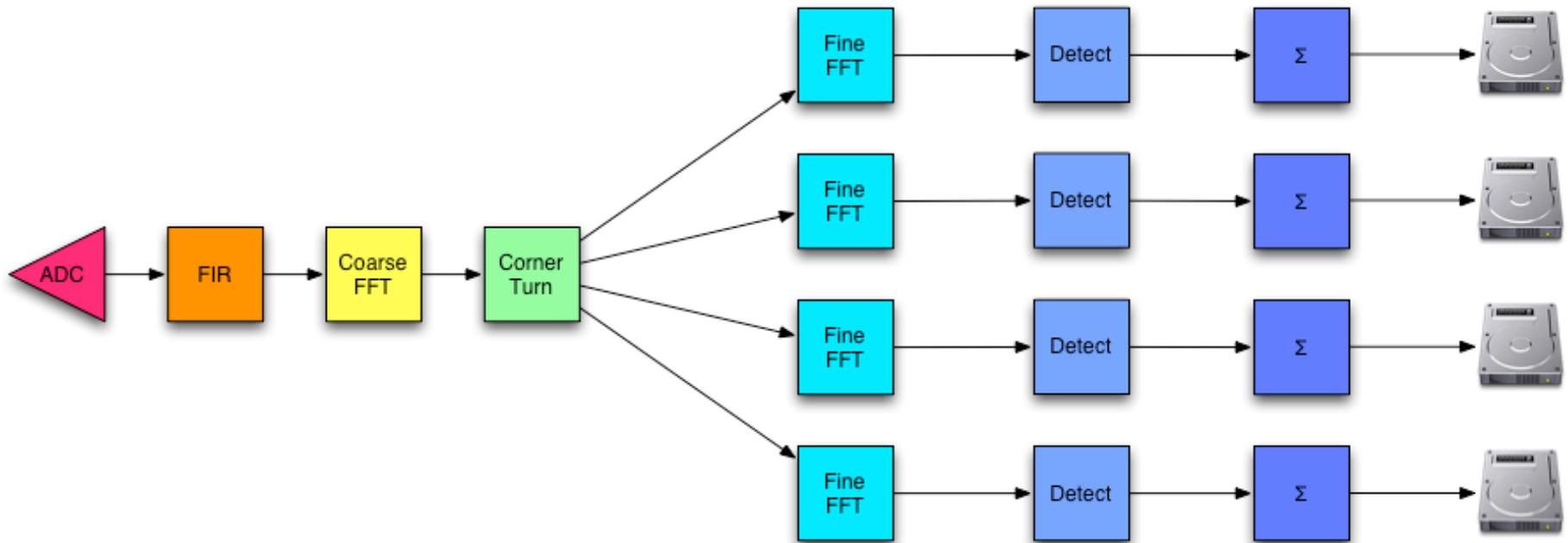
Spectrometer (1 beam, 1 pol)



Spectrometer using CPU/GPU



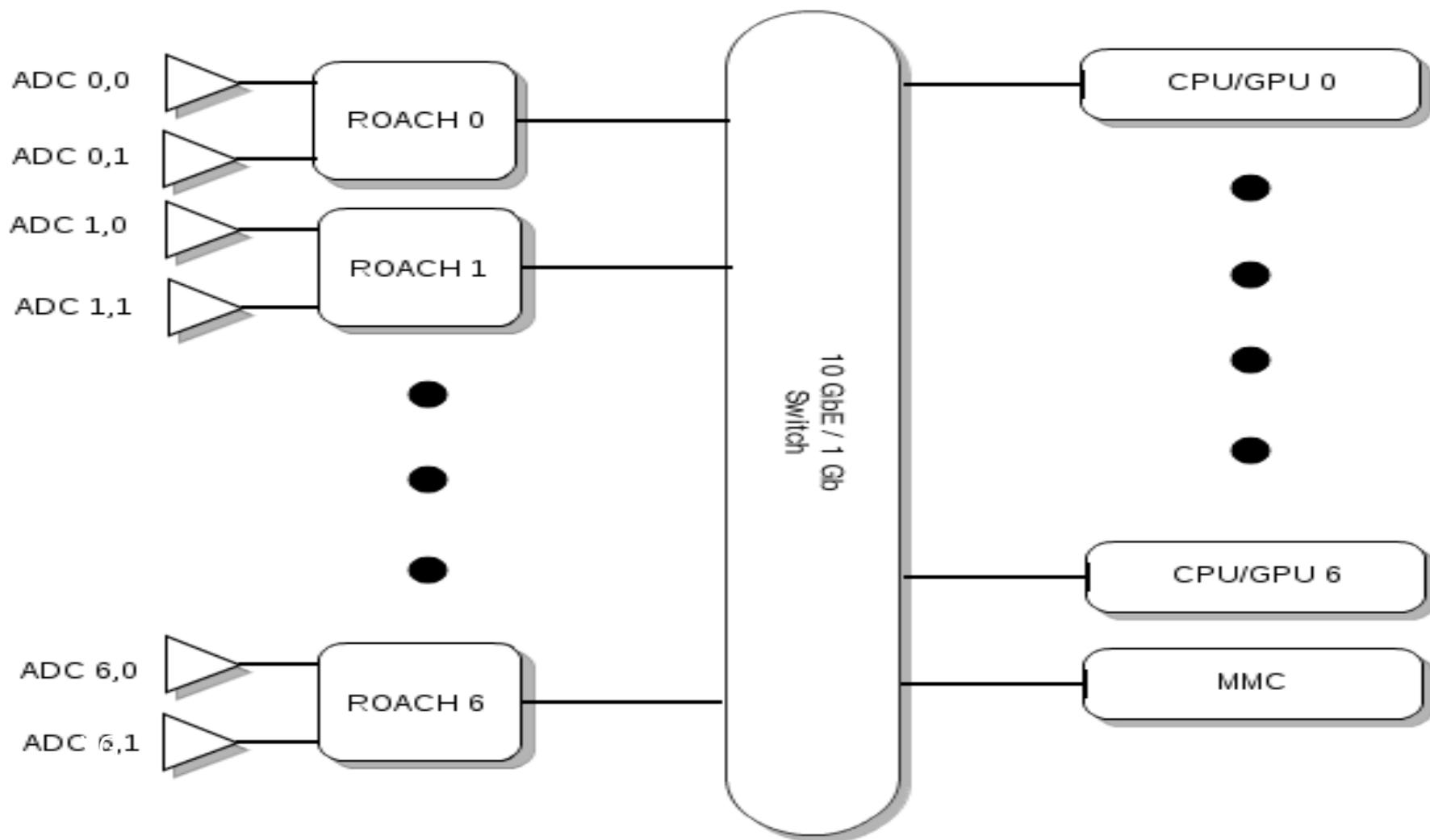
High Resolution Spectrometer





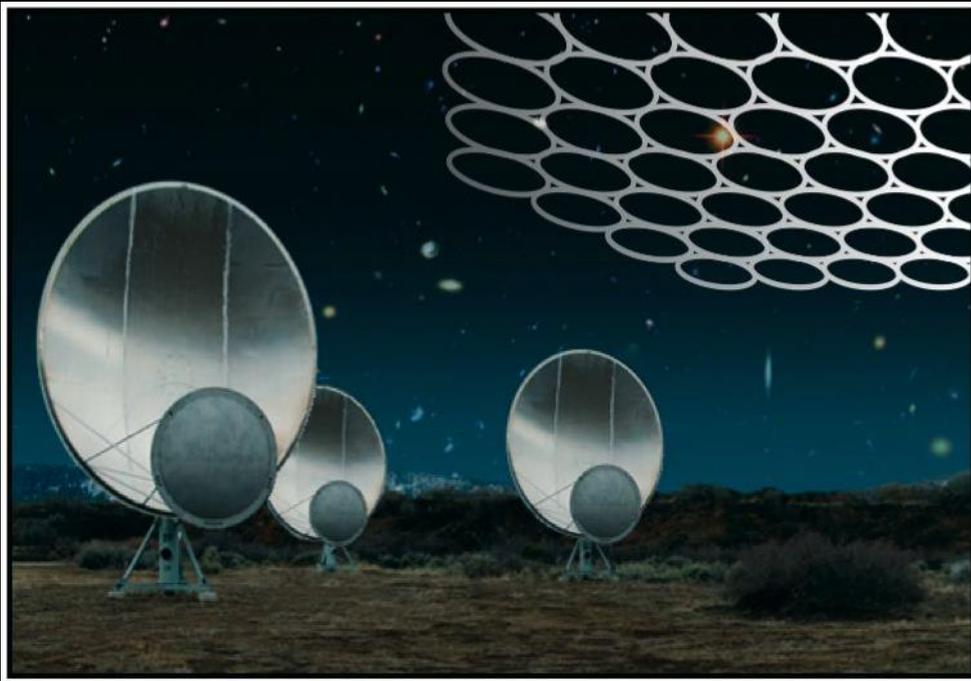
VEGAS Multi-beam Spectrometer

John Ford et al



ATA Fly's Eye Transient Instrument

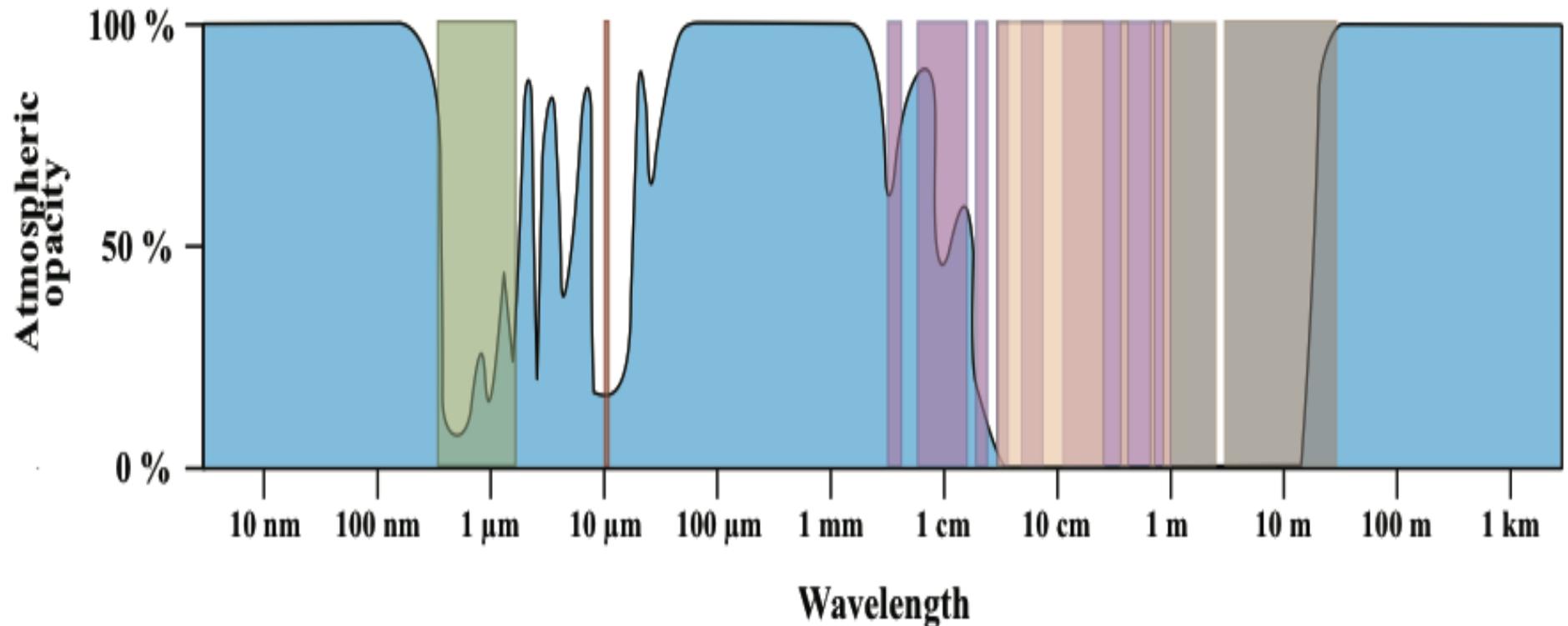
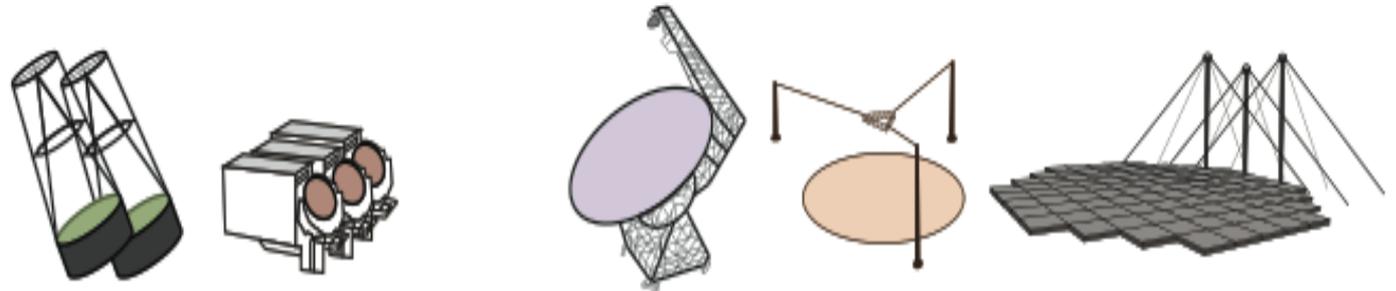
44 fast readout spectrometers
3 weeks to build



Geoff Bower, Jim Cordes, Griffin Foster, Joeri van Leeuwen, Peter McMahon, Andrew Siemion, Mark Wagner, Dan Werthimer



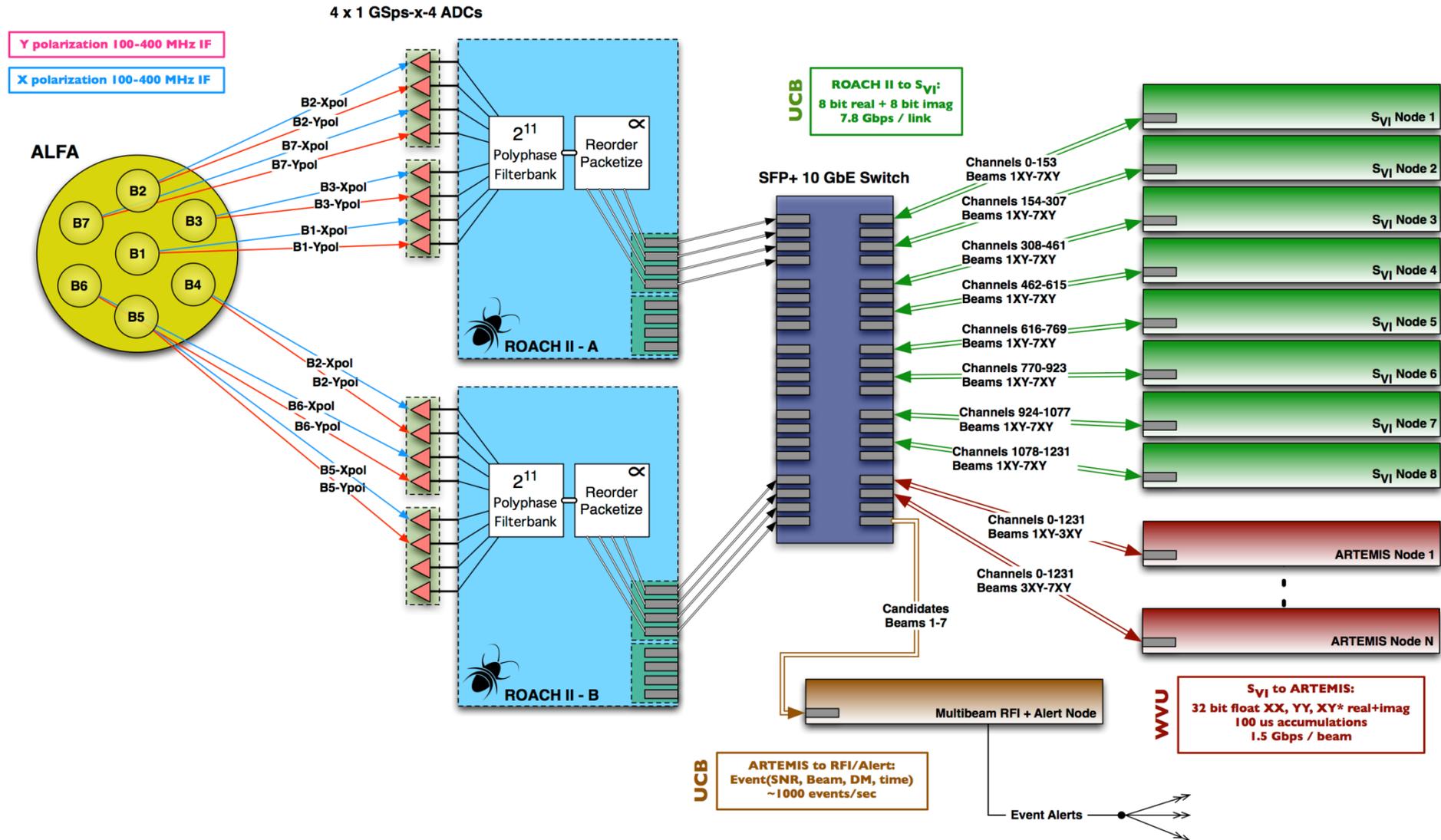
SETI Instruments (IR, Vis, Radio)



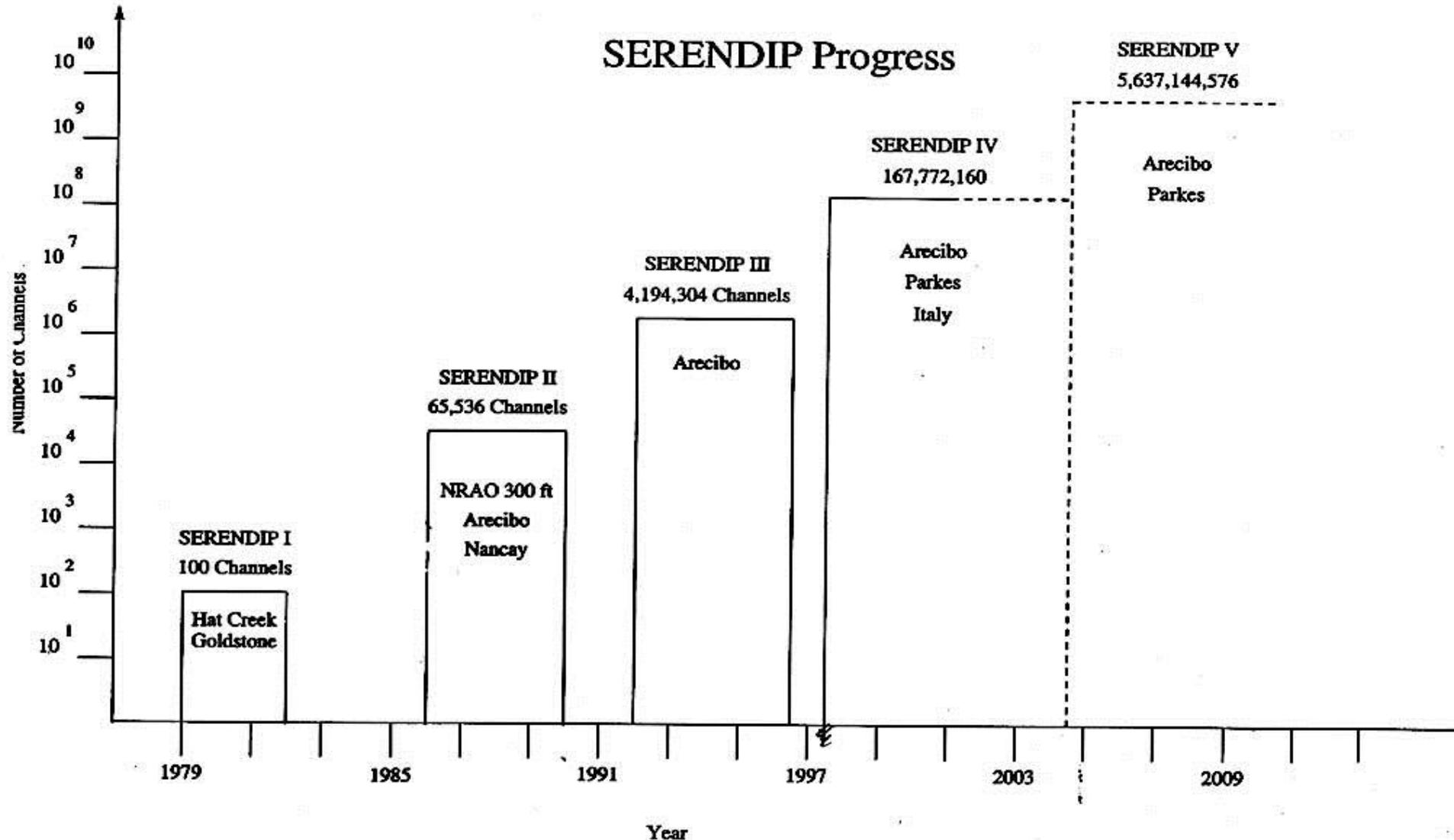
SETI and FRB search at Arecibo/GBT

SERENDIP VI and ALFABURST

Lorimer, Werthimer, Siemion, MacMahon, Dexter, Cobb, Chennamangalam, Armour, Karastergiou

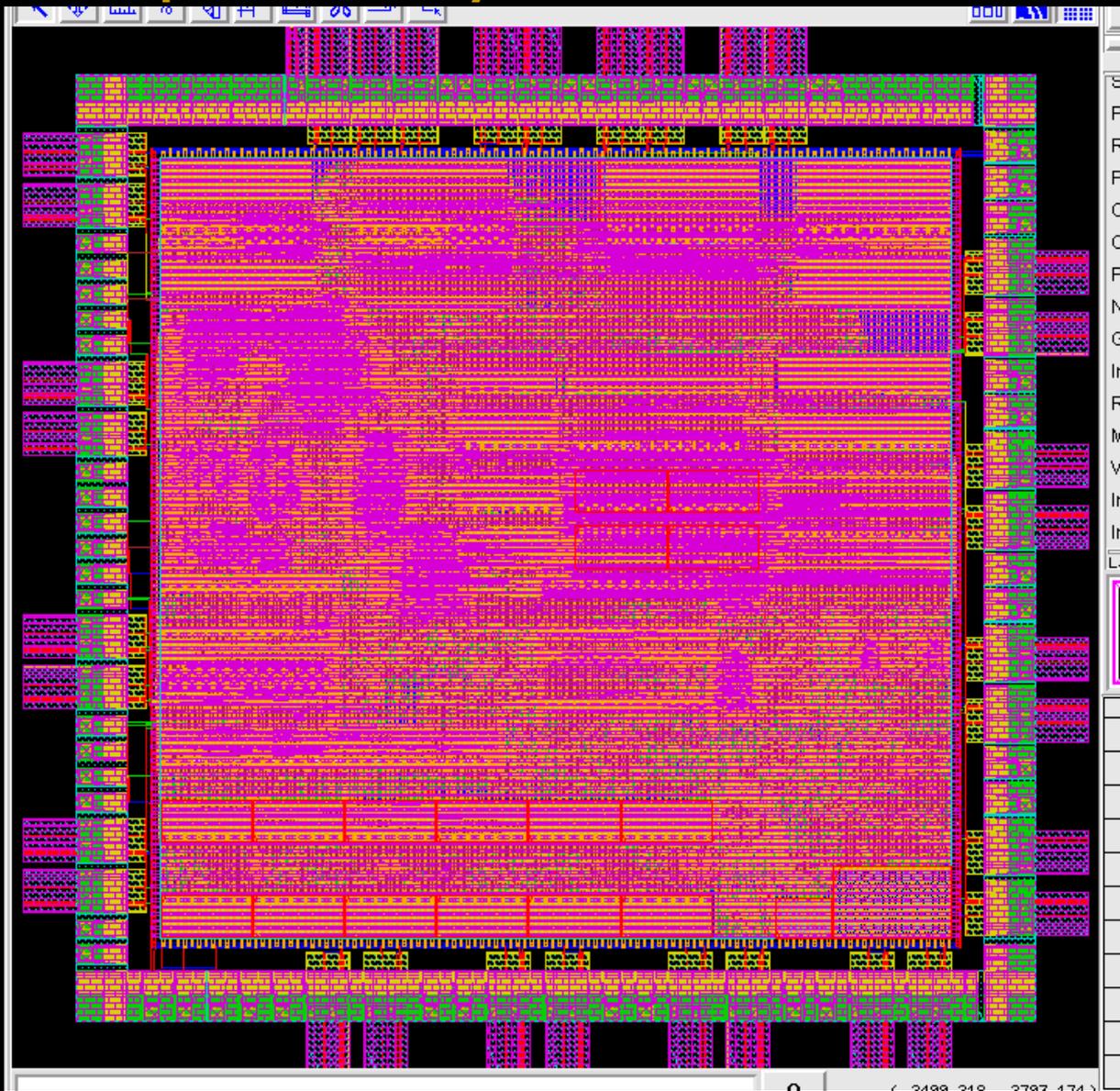


Moore's Law – Instruments using FPGA's: 2X per year (1,000,000 over 20 years)

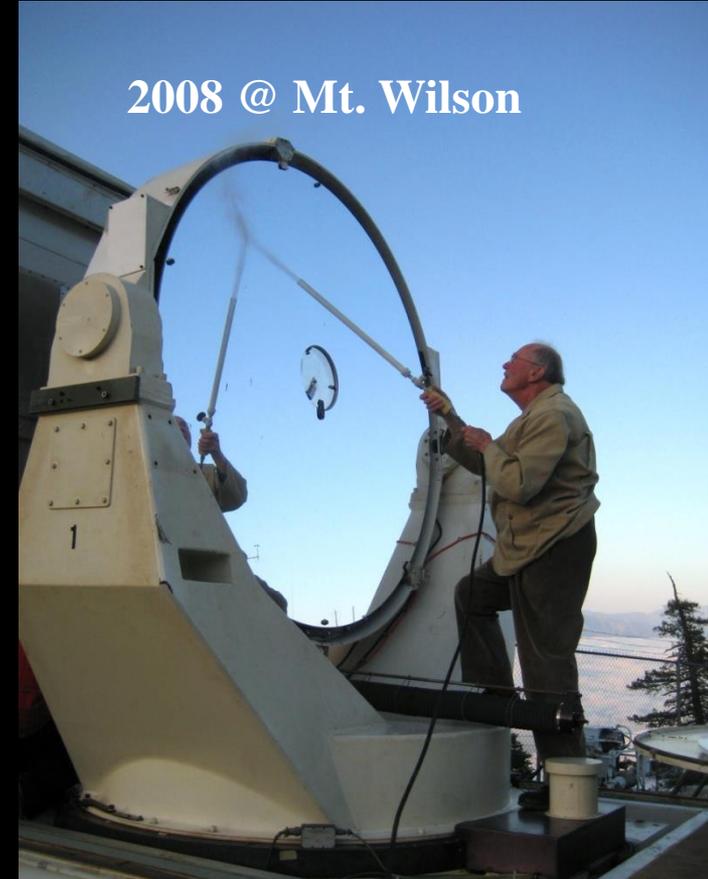


4096 channel Mars spectrometer

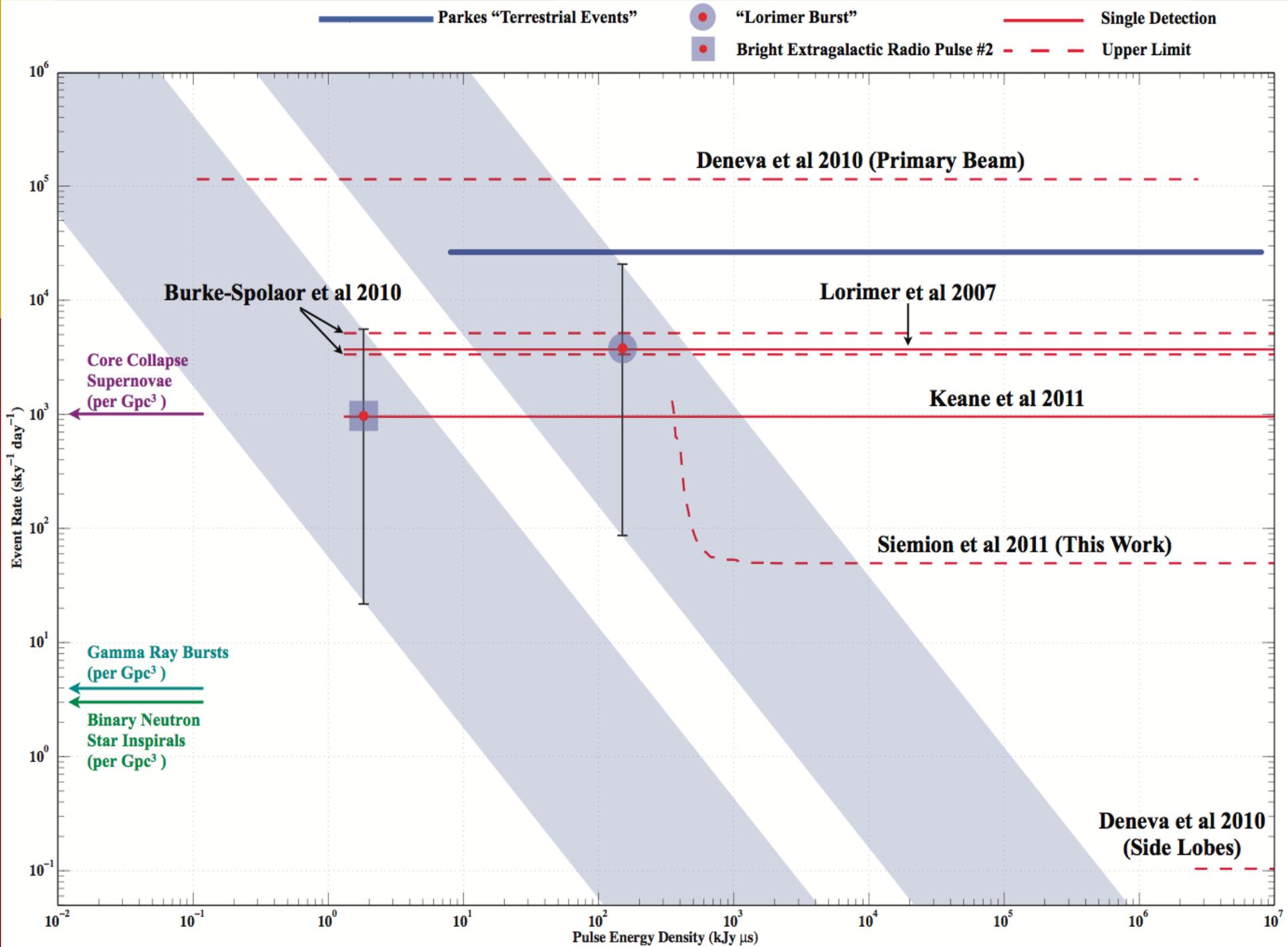
"Chip in a day" FPGA to ASIC



Infrared Spatial Interferometer heterodyne detection at 27 THz w/ CO₂ laser LOs



Mt. Wilson, CA
3 telescope system 4,8,12m early 2006
Currently ~35m triangular baselines



nature

THE BITER BIT

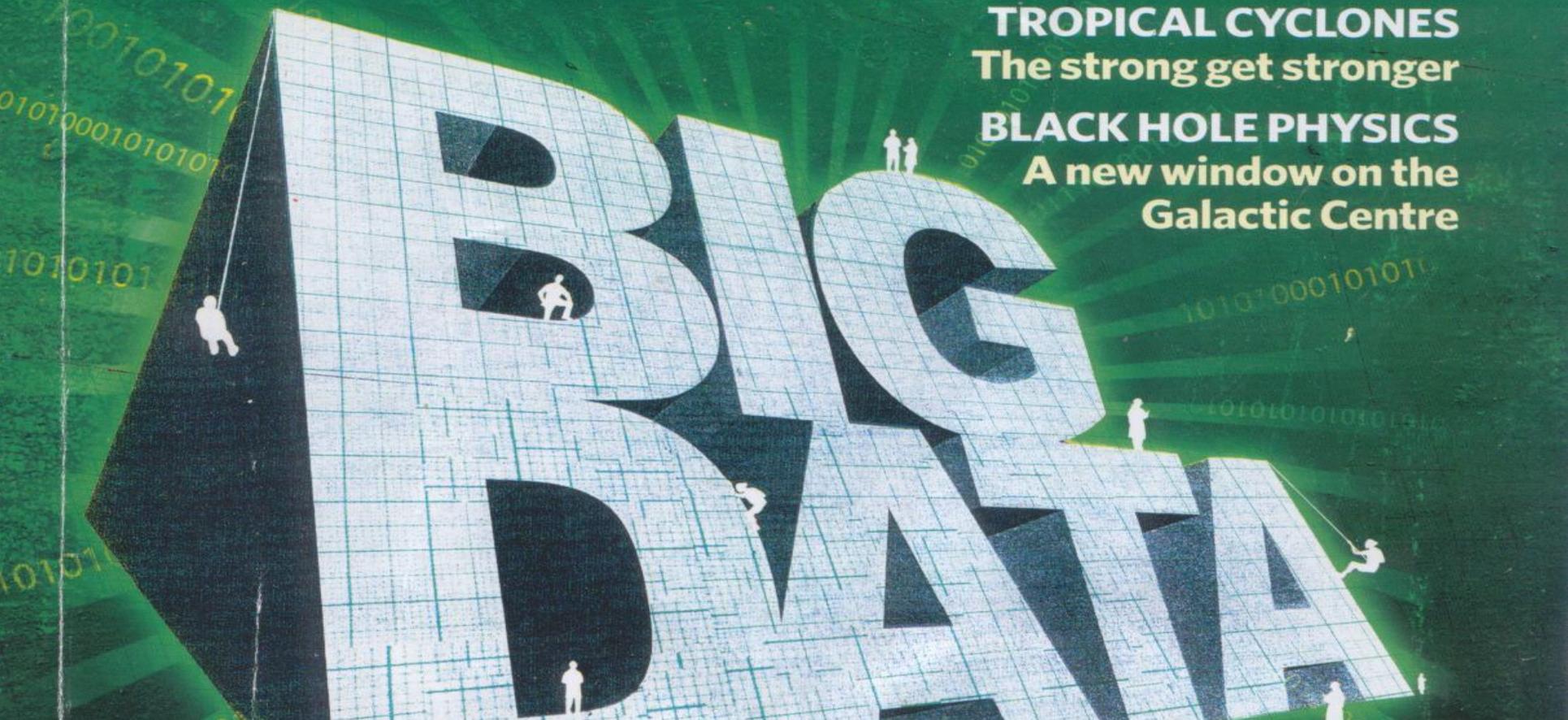
Viral infections for viruses

TROPICAL CYCLONES

The strong get stronger

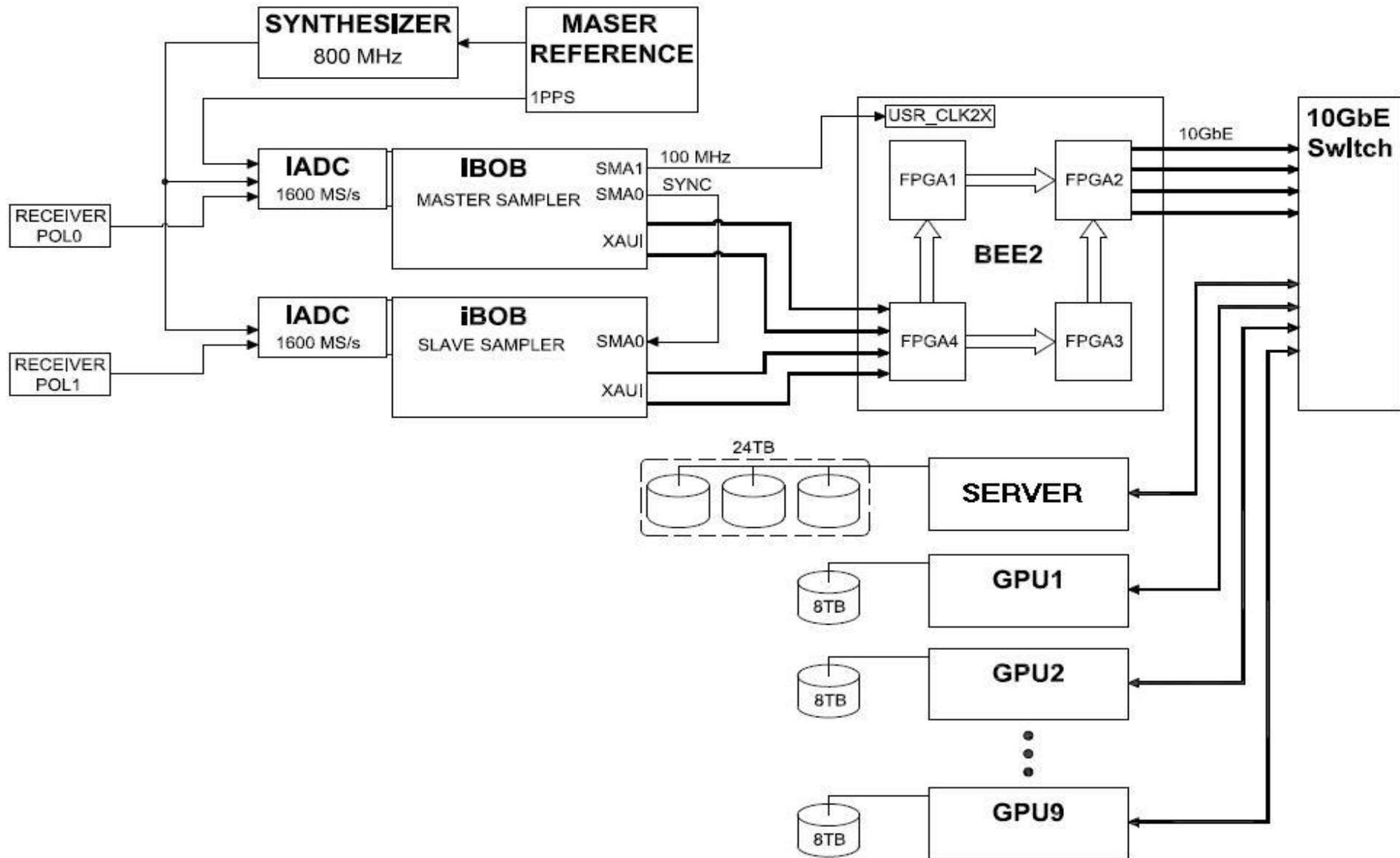
BLACK HOLE PHYSICS

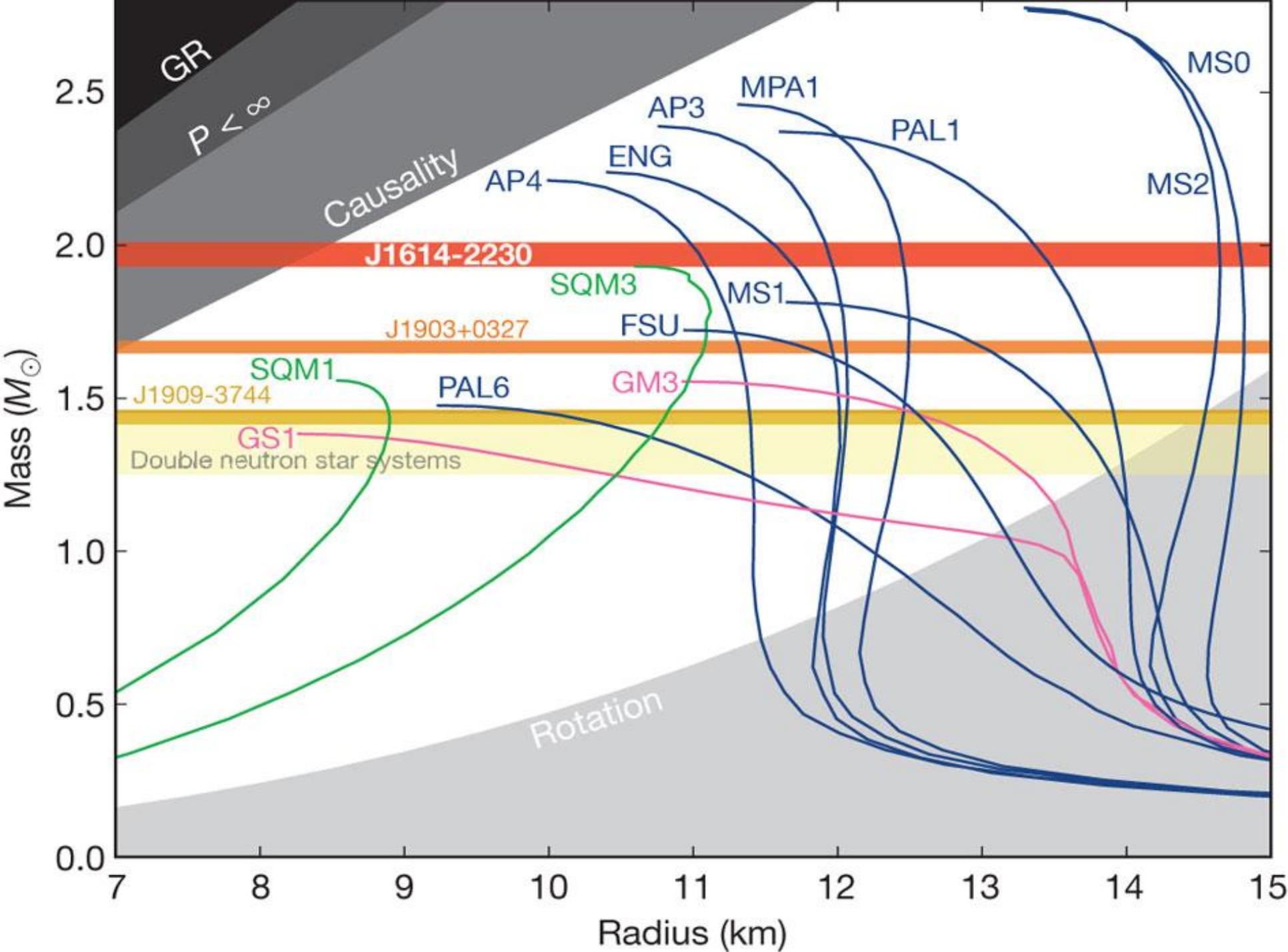
A new window on the
Galactic Centre



GUPPI Pulsar Machine: NRAO (Arecibo)

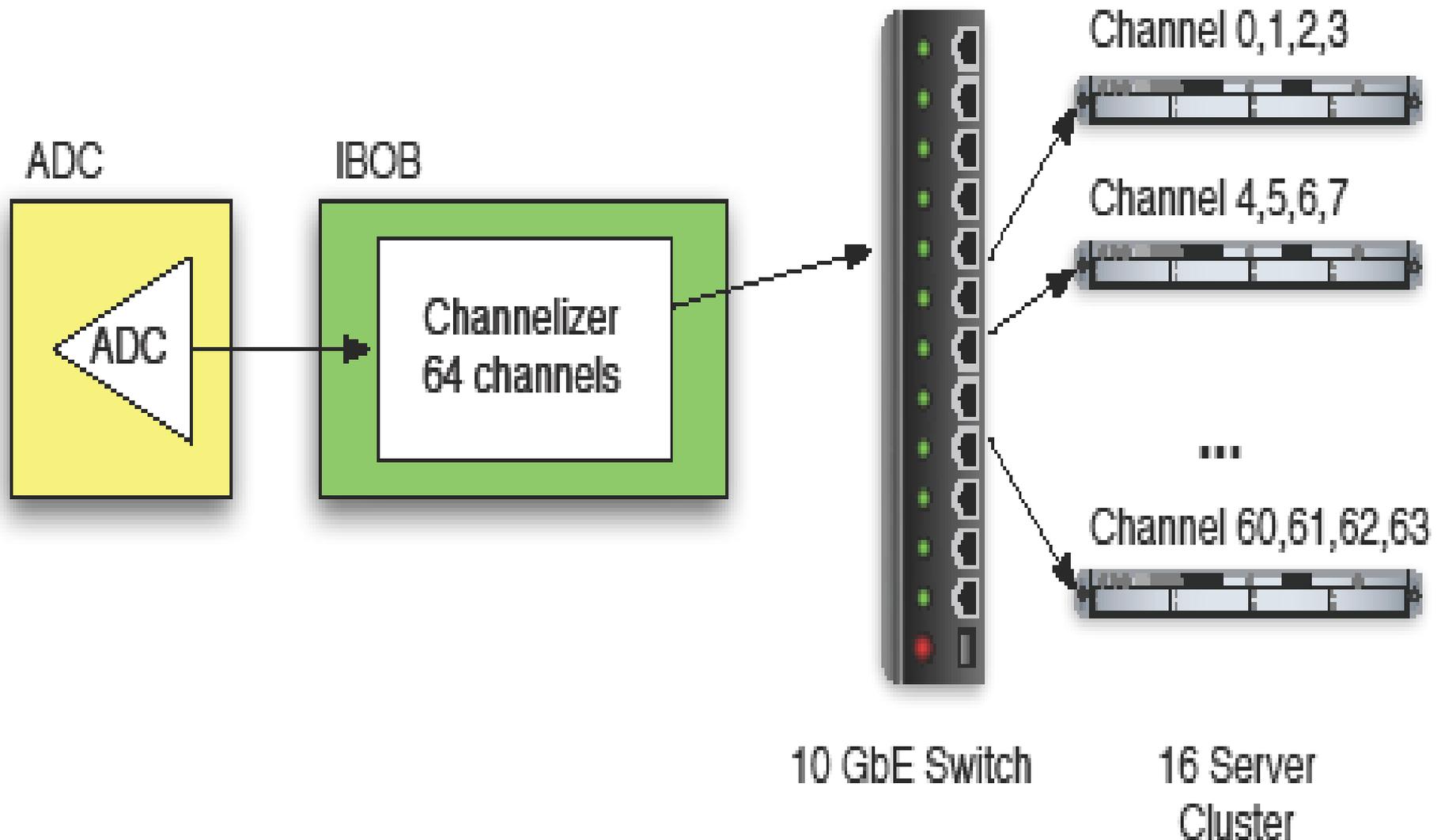
John Ford, Paul Demorest, et al



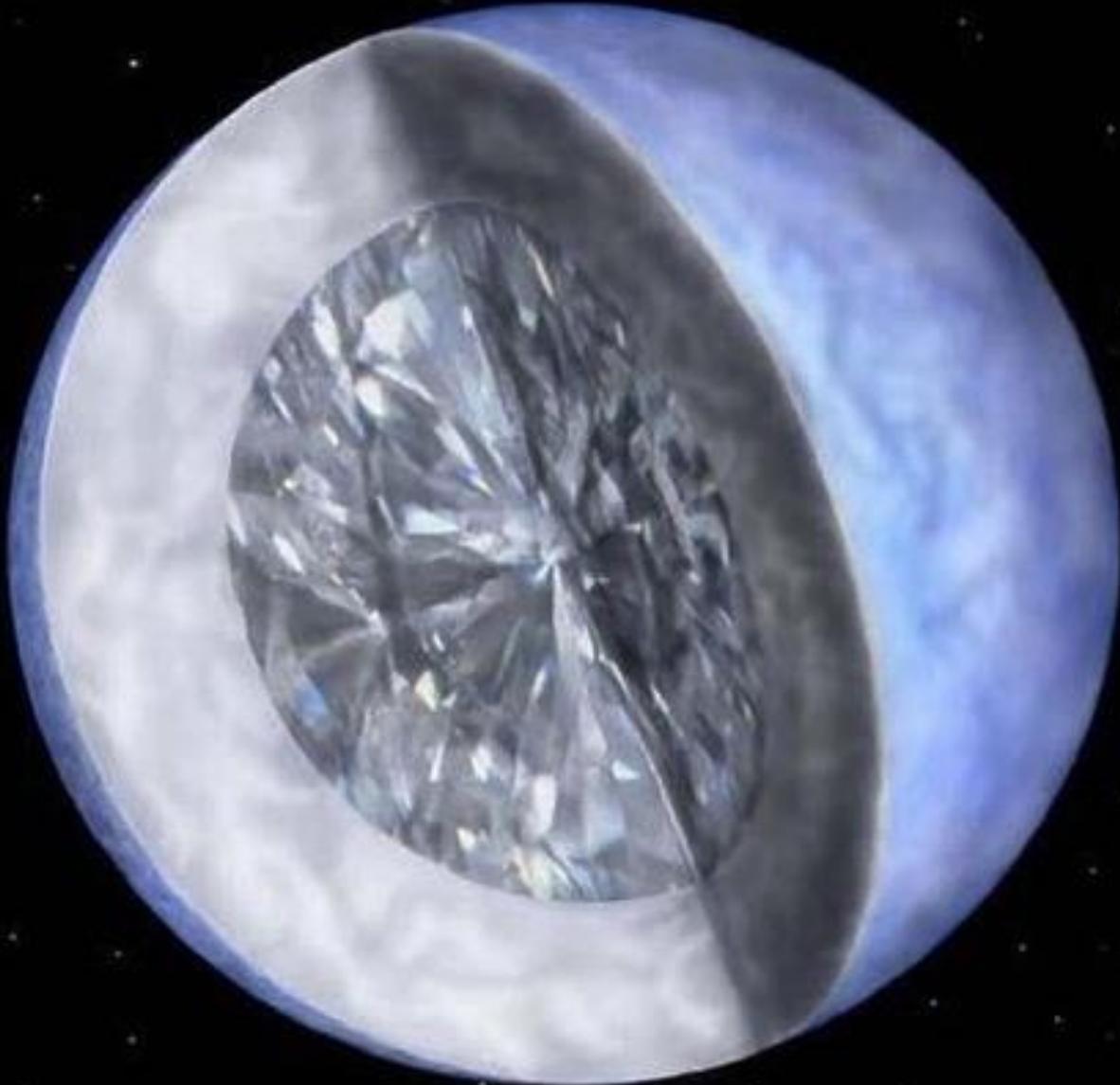


Astronomy Signal Processor

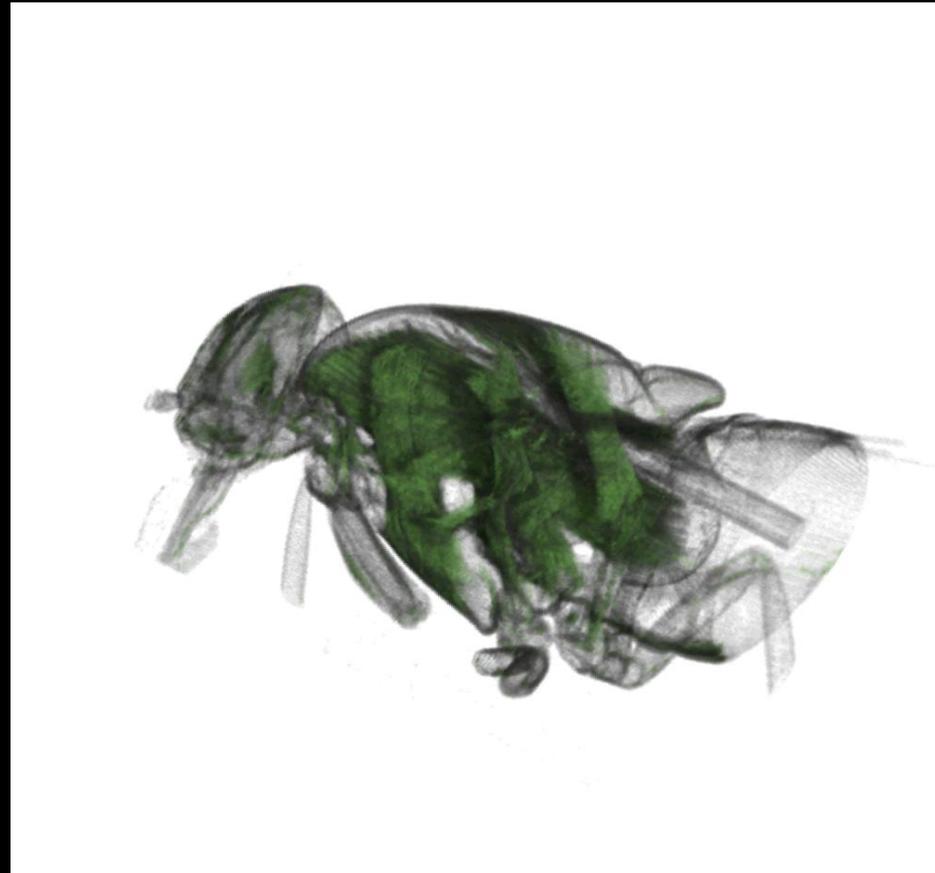
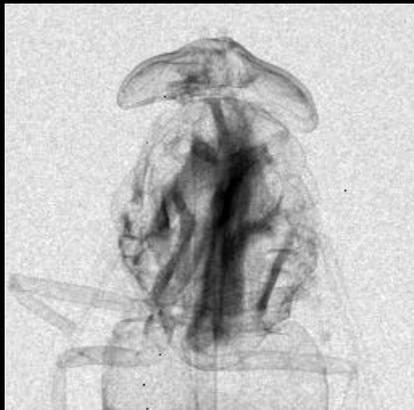
Terry Filiba, Peter McMahon



Diamond Planet: Matthew Bailes et al



Neutron radiography : MCP, Roach

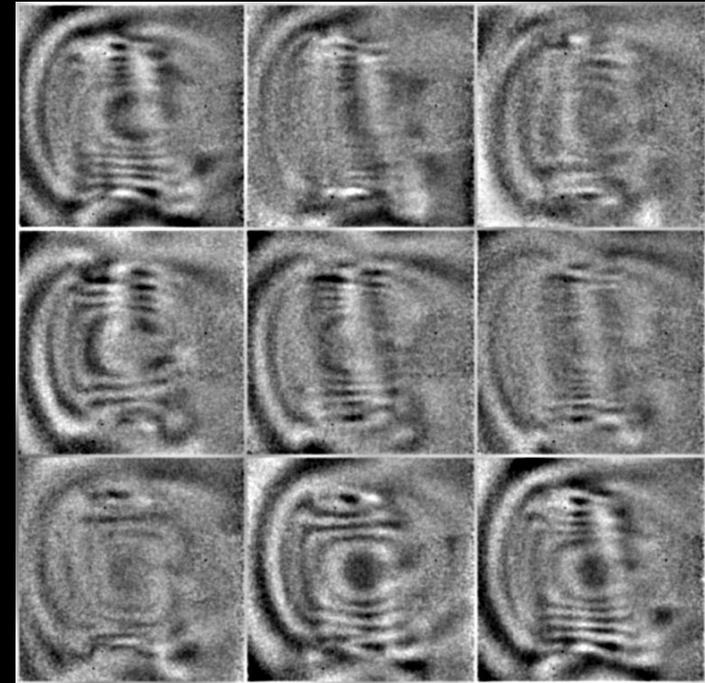
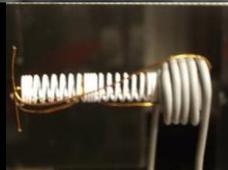
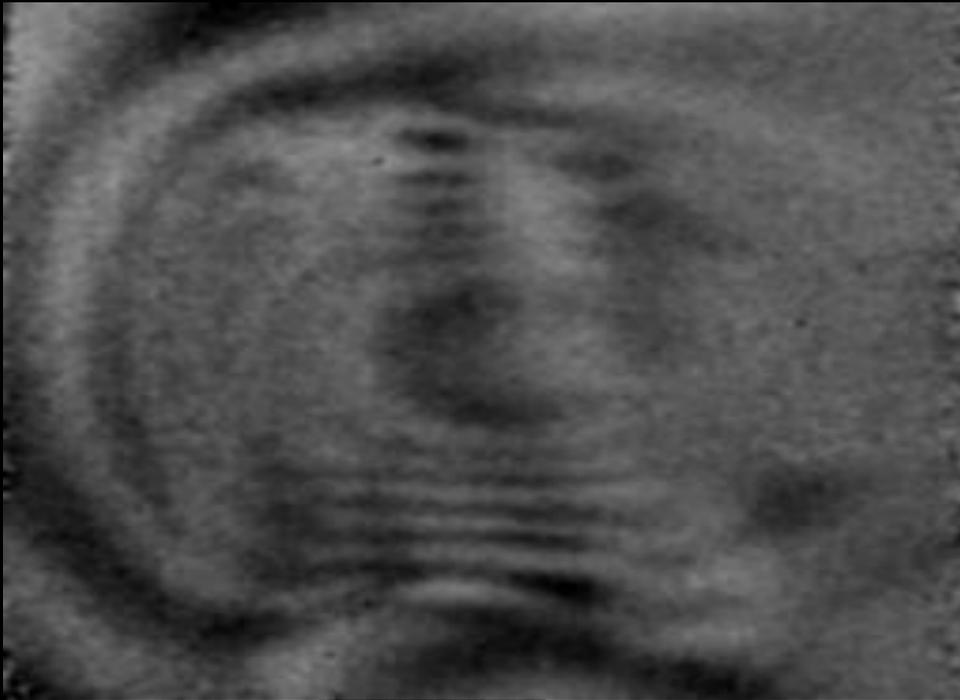


ICON beamline.

Tissues with different neutron absorption coefficient are depicted by different colors. 201 tomographic projections taken with 140 s image acquisition time each.

Dynamic magnetic field imaging:

3 kHz field: 10A AC
current
10 μ s time slices



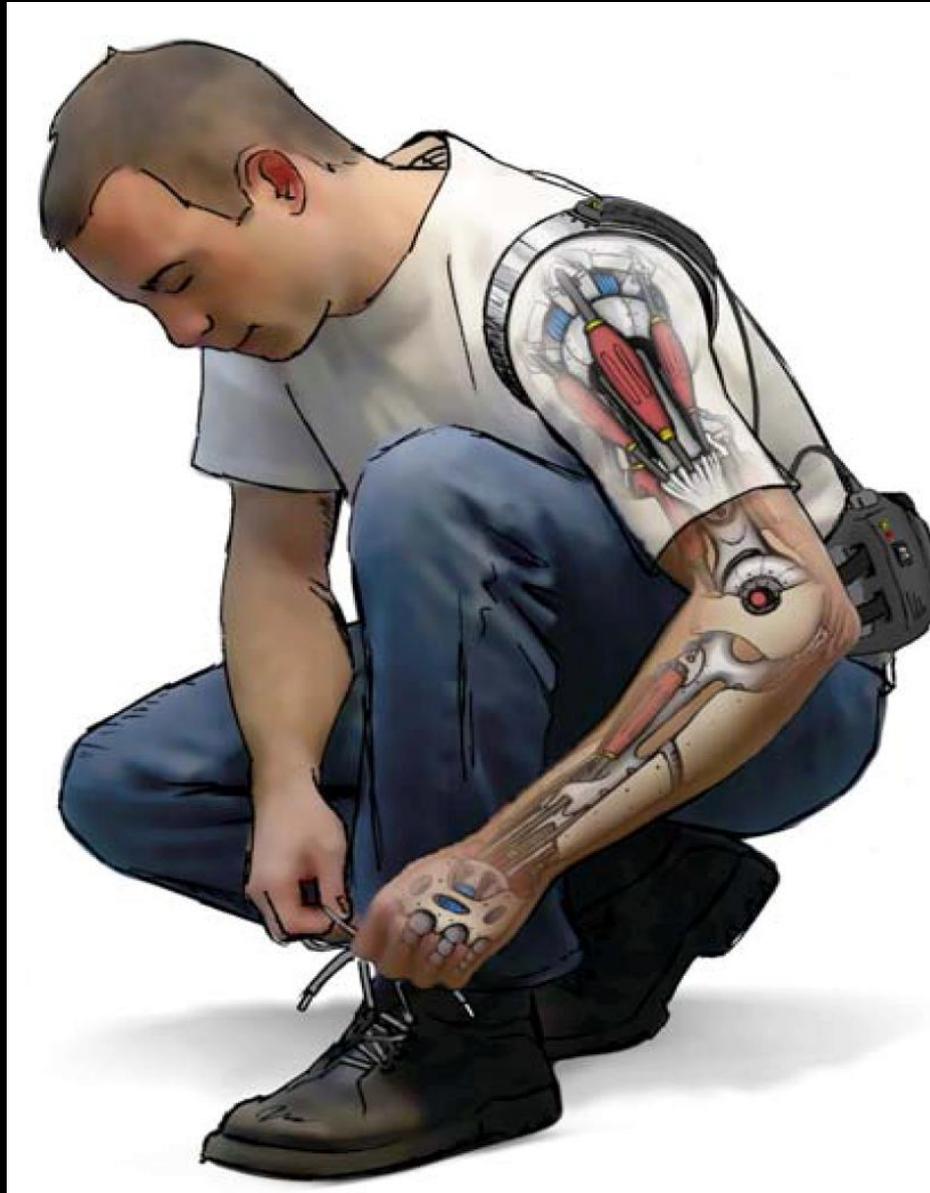
Magnetic field produced by 3 kHz
AC current in a coil imaged

Brain Readout using Roach and Casper Tools

10 Mbit/sec - (Borg?)



Prostheses Control



Microwire Neural Implants



Correlators and Beamformers

Correlator Ops and Bits

$$\begin{aligned}\text{CMAC/sec} &= \text{bandwidth} \times \text{Nantenna}^2 \\ &= 1 \text{ GHz} \times 3000^2 \\ &= 1\text{E}16 \text{ CMACS per beam}\end{aligned}$$

$$\begin{aligned}\text{Bits/sec} &= \text{bandwidth} \times \text{Nantenna} \times 16 \text{ bits} \\ &= 1 \text{ GHz} \times 3000 \times 16 \\ &= 50 \text{ Tbit/sec per beam}\end{aligned}$$

Correlator References

Thompson, Moran, Swenson, 2nd edition

Interferometry and Synthesis in Radio Astronomy

Parsons, A Scalable Correlator Architecture Based
on Modular FPGA Hardware and Data Packetization

<http://casper.berkeley.edu/wiki/Papers>

<http://casper.berkeley.edu/>

CASPER Correlator Collaboration

Allen Telescope Array (90 uS imaging)

PAPER (Epoch of Reionization)

Carma Next Generation

MeerKAT/SKA South Africa

GMRT next gen

Bologna

ISI (Infrared) – 6 Gbps (3 GHz)

SKADS (Oxford)

SMA next gen (CFA, ASIAA)

MIT FFT direct imaging correlator

FASR?, Baryon Acoustic Oscillation ?

LEDA (CFA GPU X engine)

Berkeley Correlator Team

- Dan Werthimer (28 years correlator design)
- Matt Dexter (20 years correlator design)
- David McMahon (10 years correlator design)
- Aaron Parsons (6 years correlator design)
- Rick Raffanti (ADC and RF/analog board designer – 30 years)
- Dave Deboer (project manager)
- Terry Filiba (EE grad student – F engine)
- Andrew Siemion (Astr grad student – correlators, transient, pulsars, SETI)
- Suraj Gowda (EE grad student – high speed FGPA tools)
- Hong Chen (Astr. Undergrad – parameterized FPGA designs)
- Mark Wagner (staff scientist – instrument designer)

Correlator Technologies

Software Correlators (DiFX – Adam Deller)

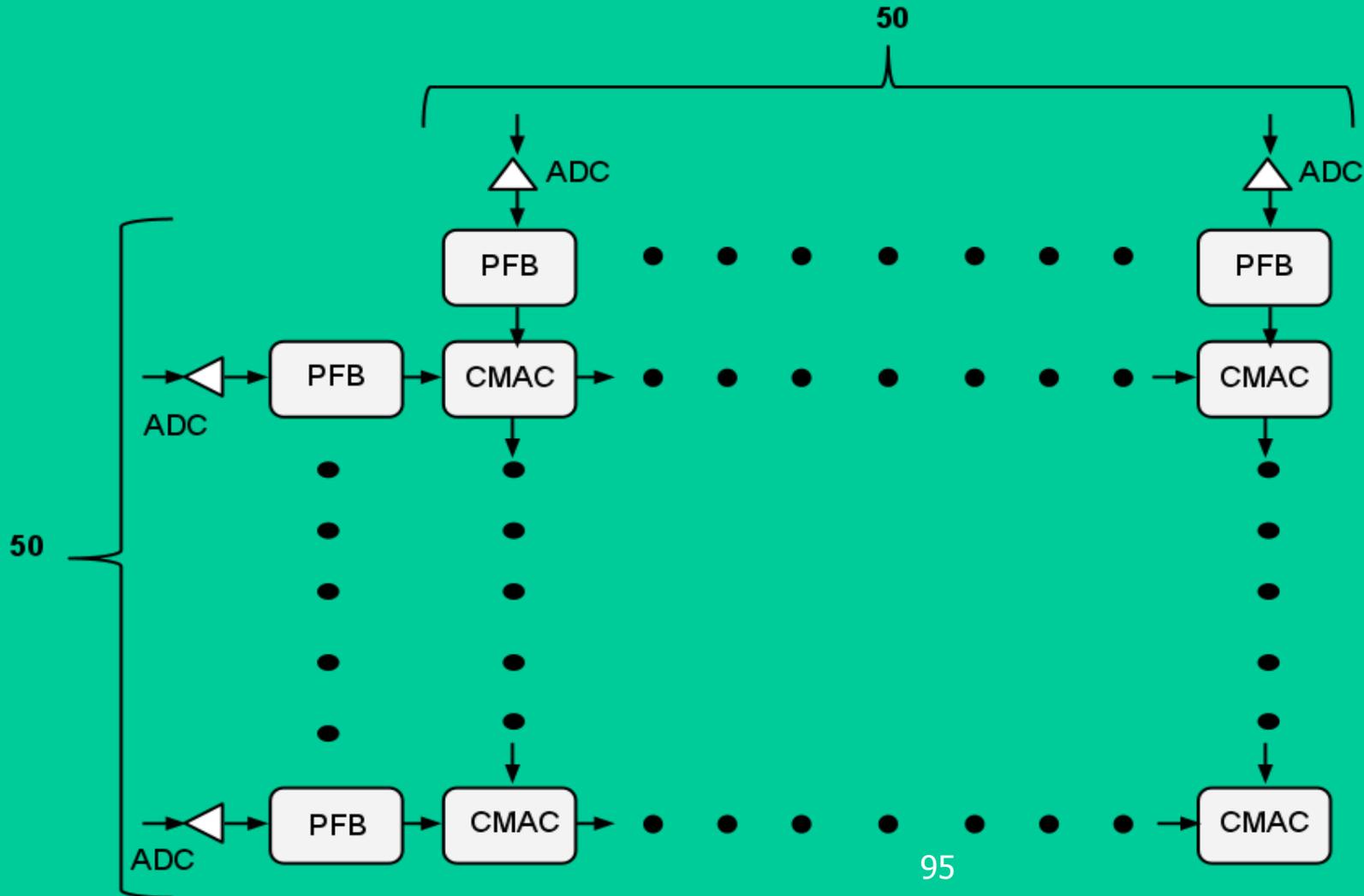
GPU Correlators (CASPER, Xgpu – Mike Clarke)

FGPA Correlators (CASPER, F and X engines)

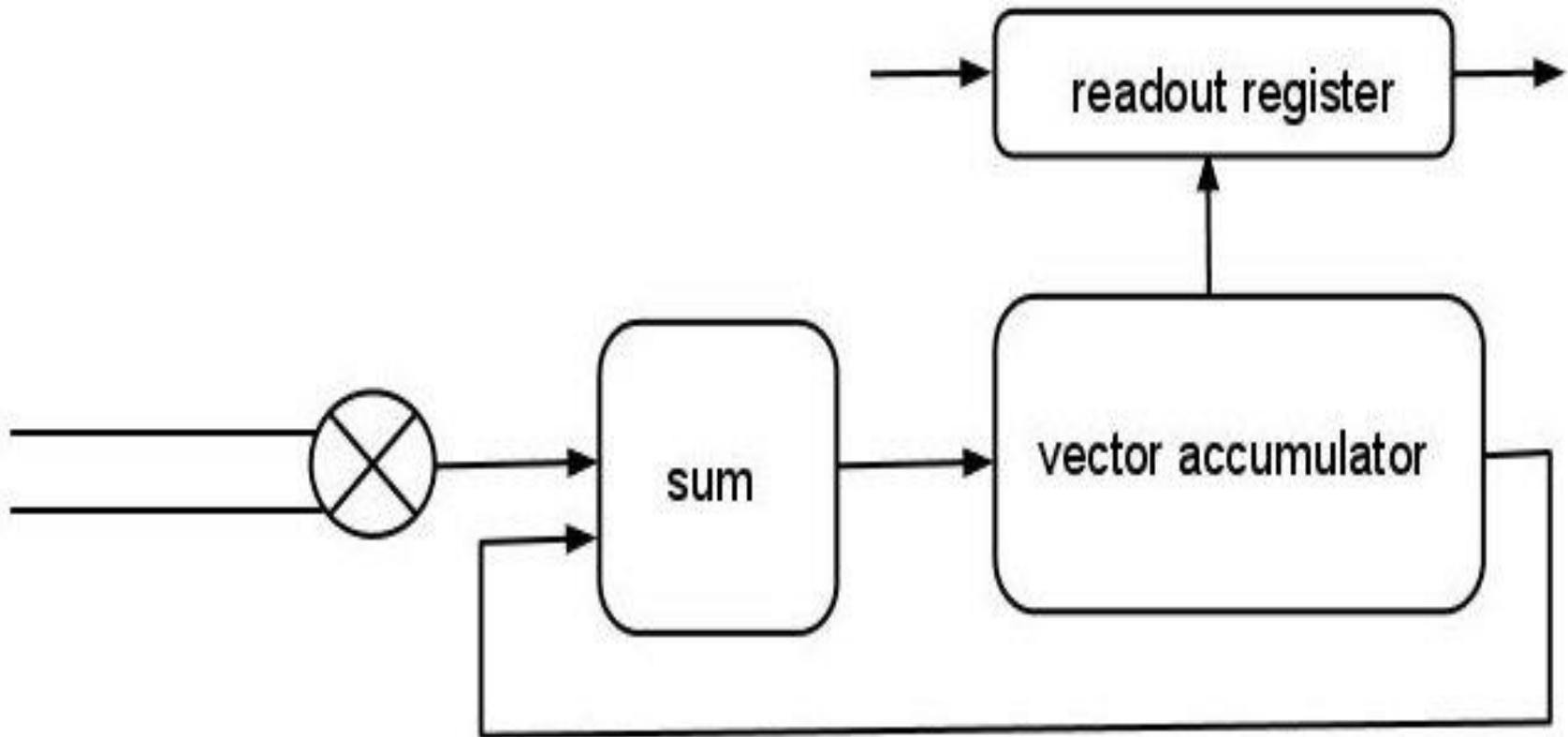
ASIC Correlators (NRAO, DRAO, JPL...)

What ELSE ??? (Intel Phi??)

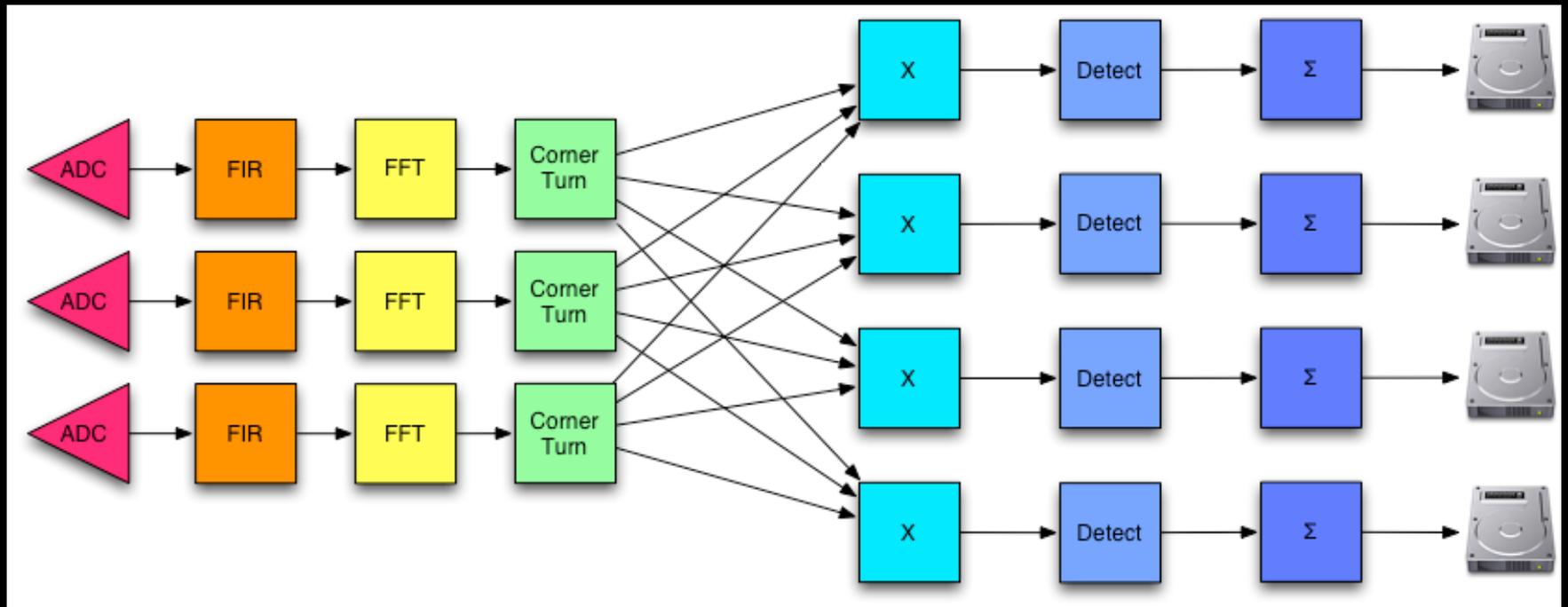
Small Correlator (one board)

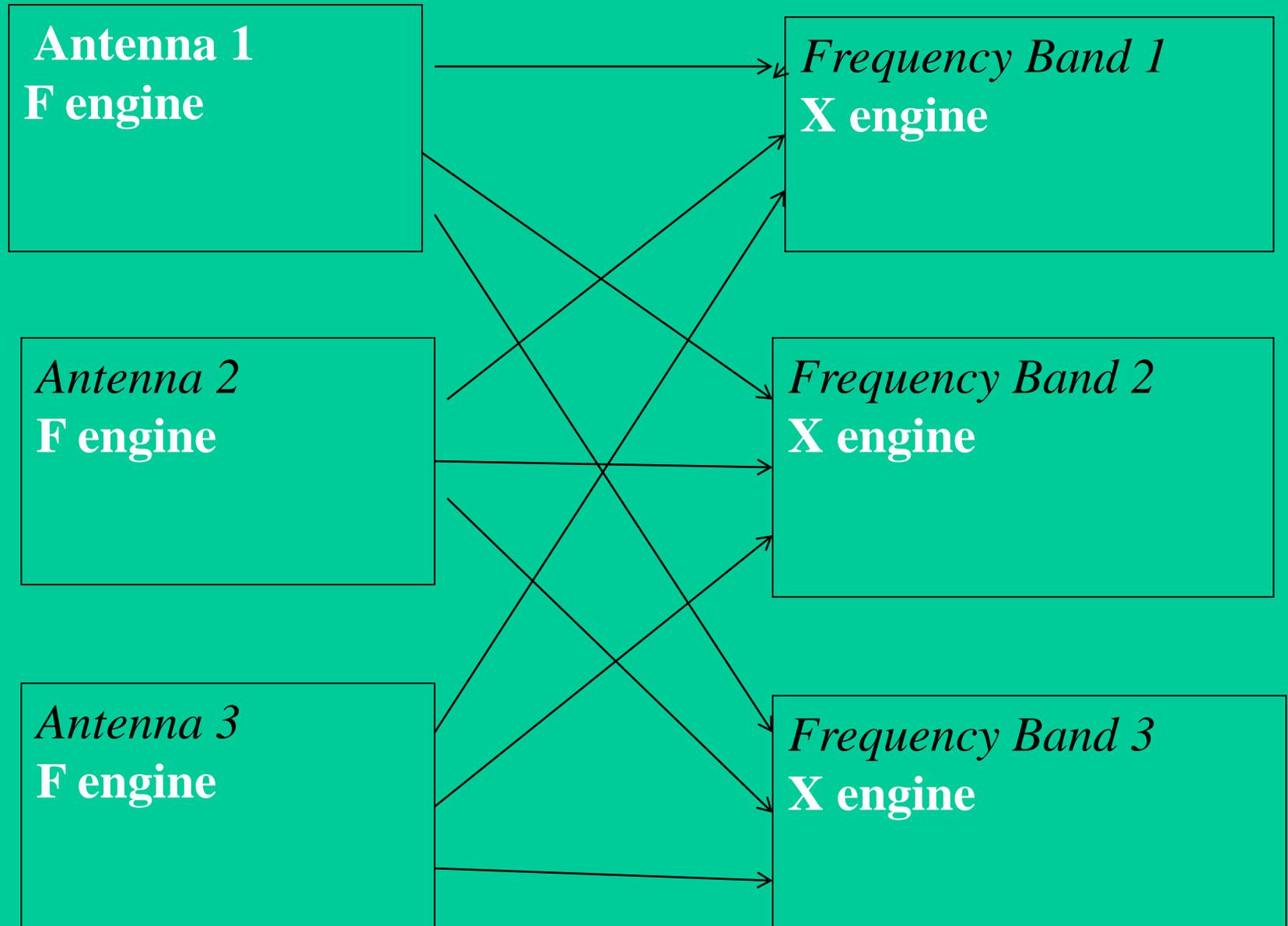


CMAC Complex Multiplier Accumuator

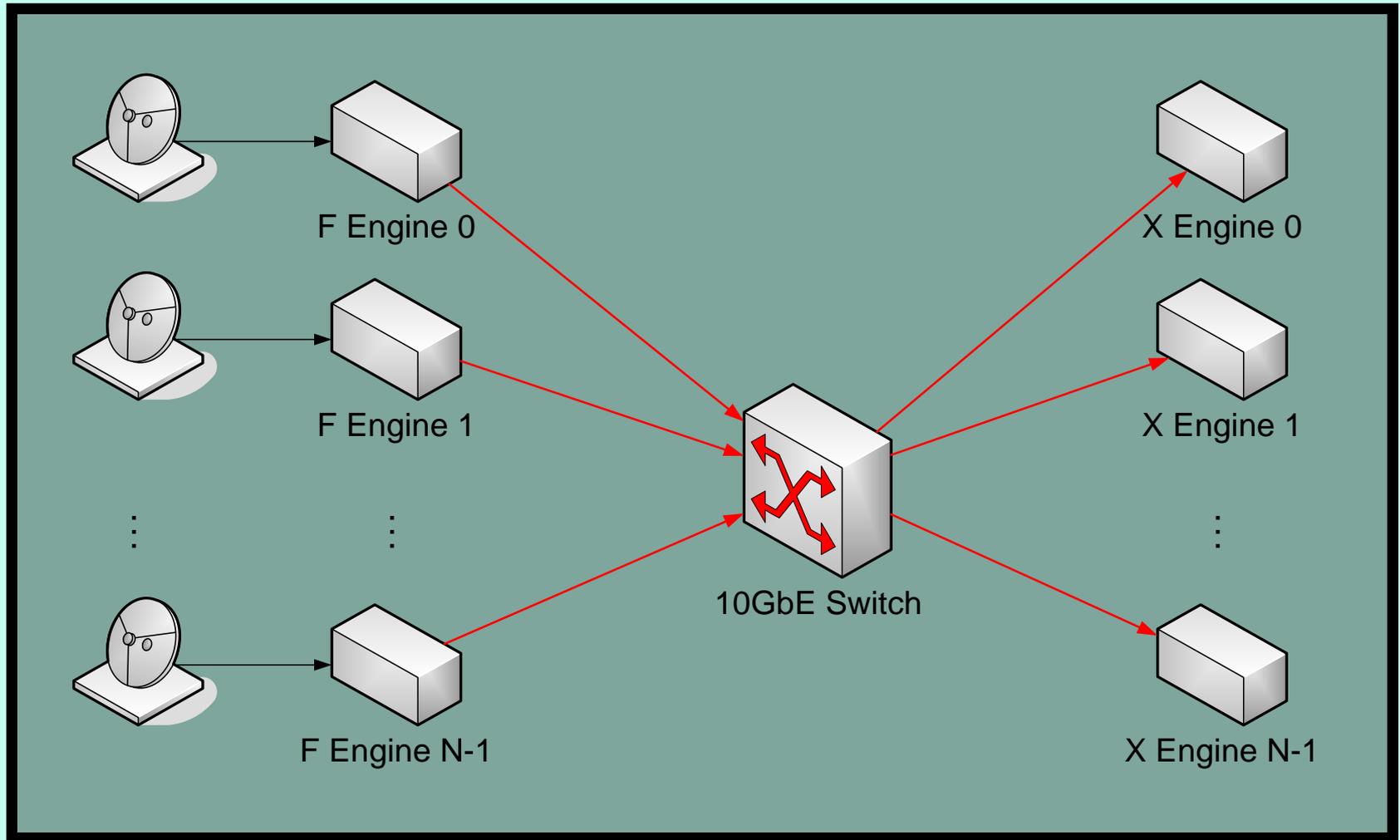


FX Correlator

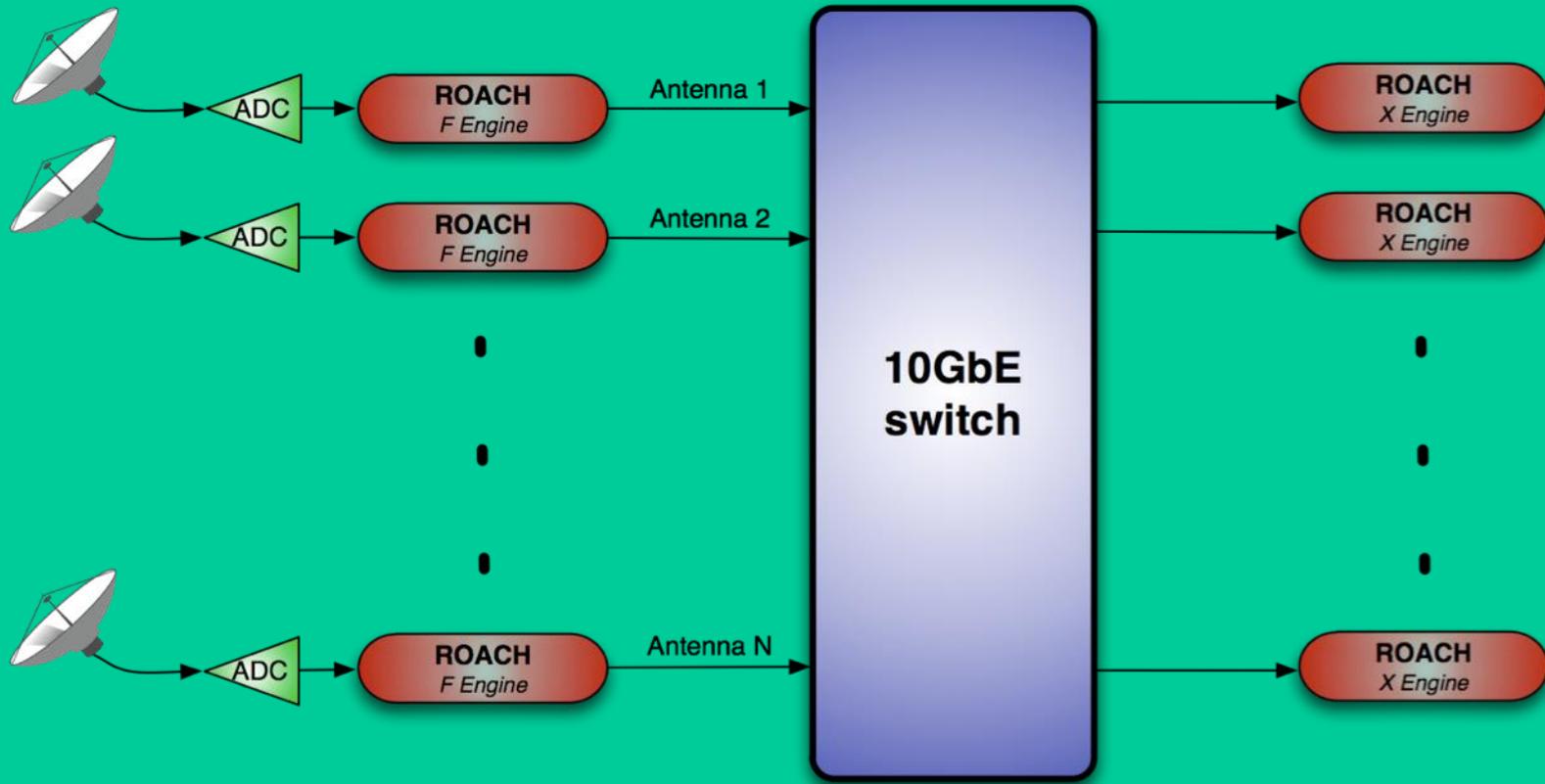


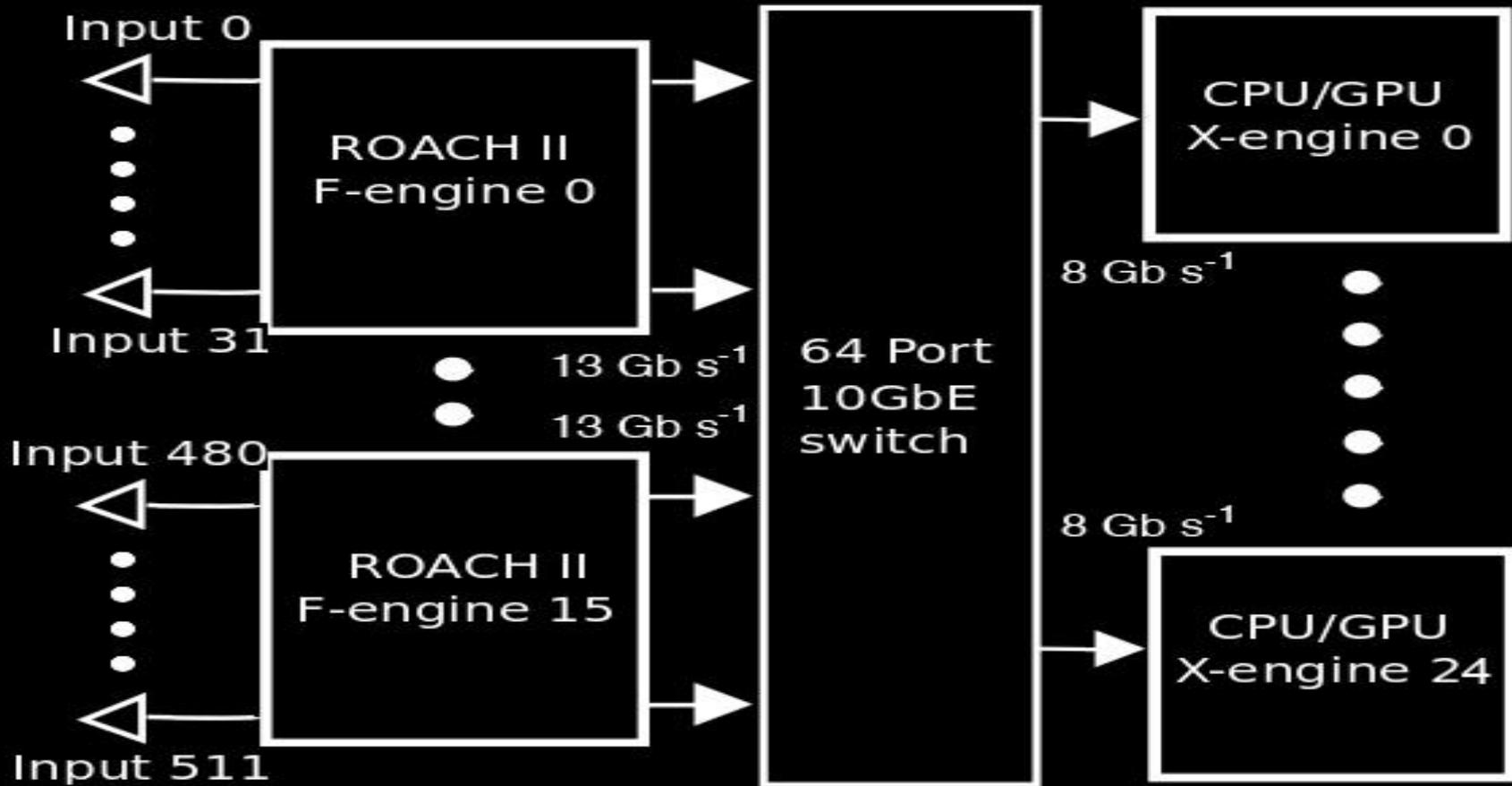


CASPER FXB Correlator/Beamformer (correlator needed to calibrate beamformer)

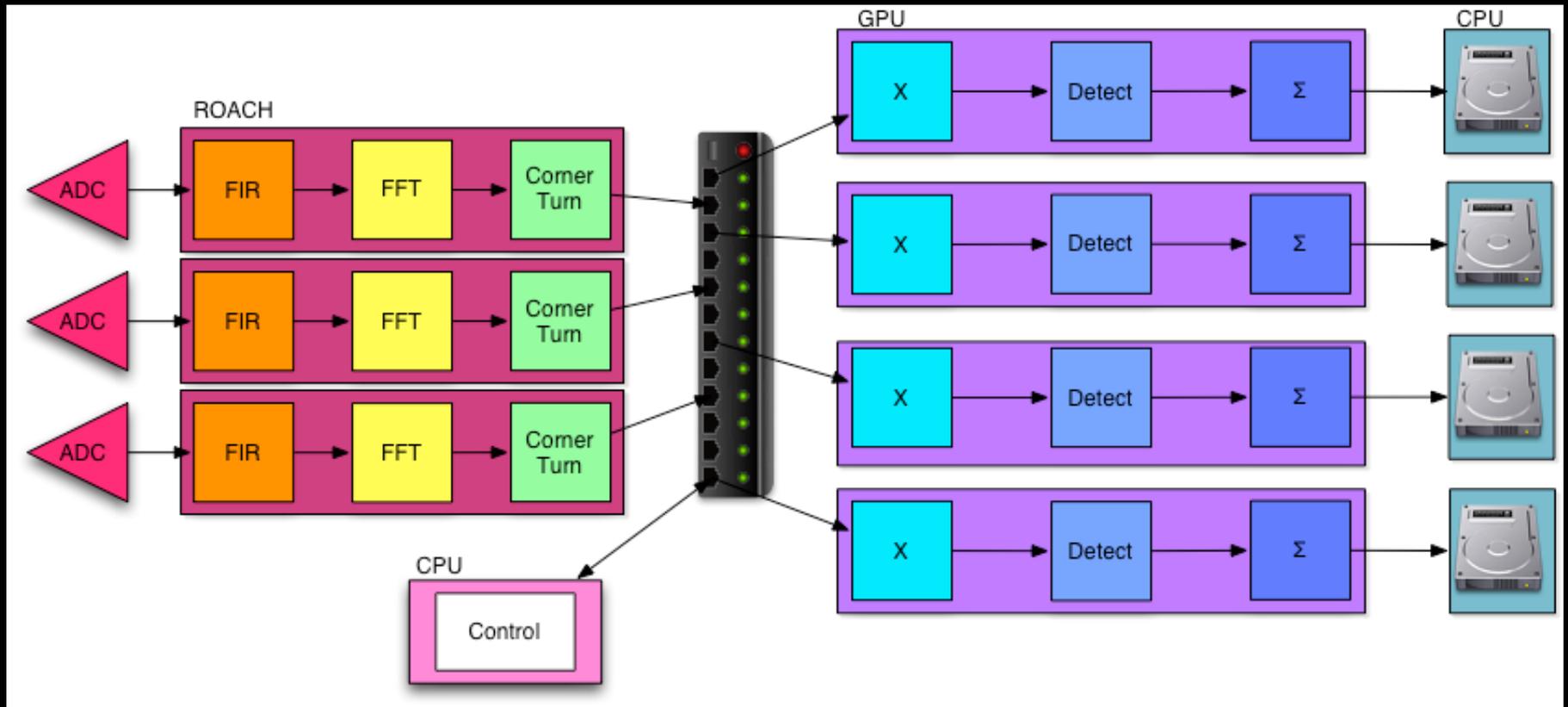


CASPER FPGA Packetized Correlator

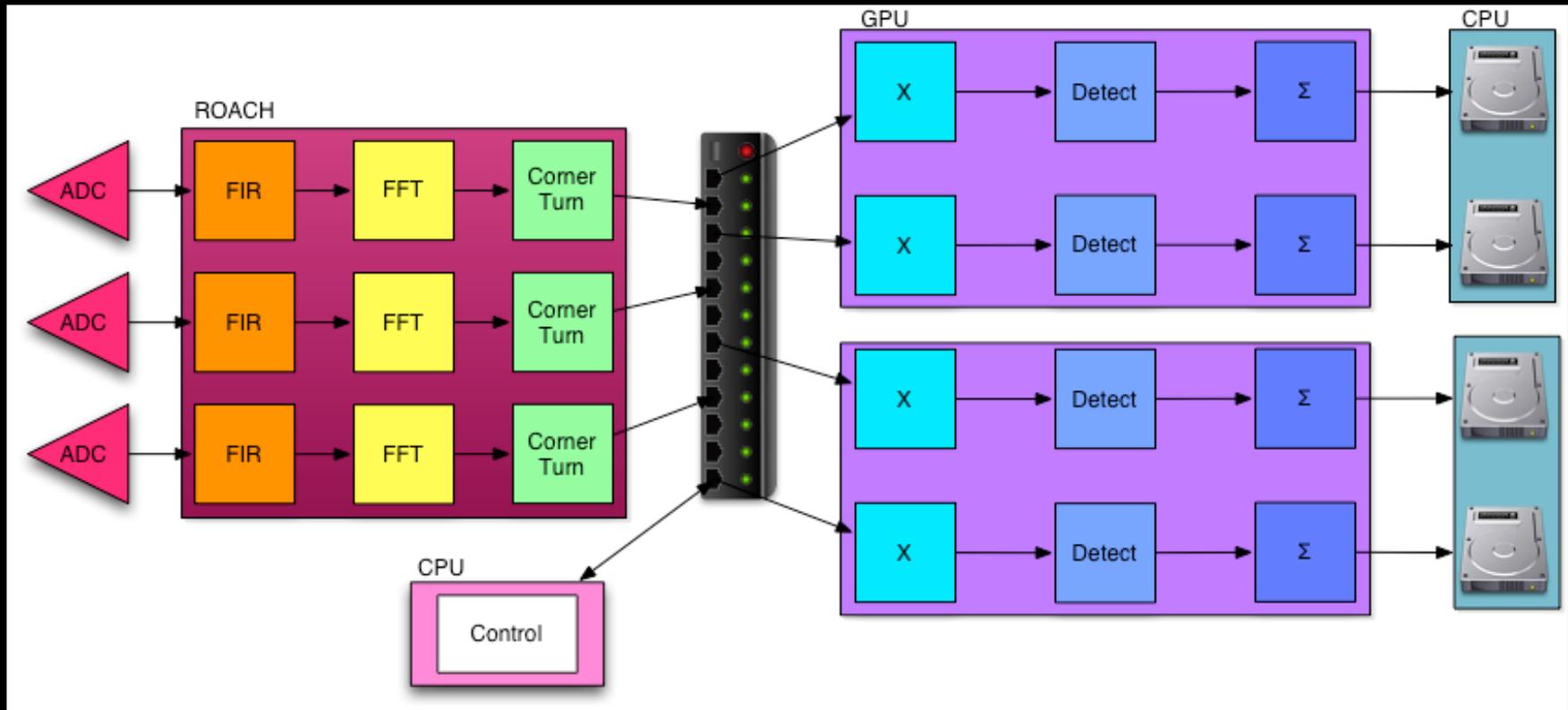




Packetized FX Correlator



Heterogeneous Correlator



Data Transport Software for Heterogeneous Instrumentation

PSRDADA – Australia, Kocz et al

HASHPIPE – NRAO, UCB, D. MacMahon

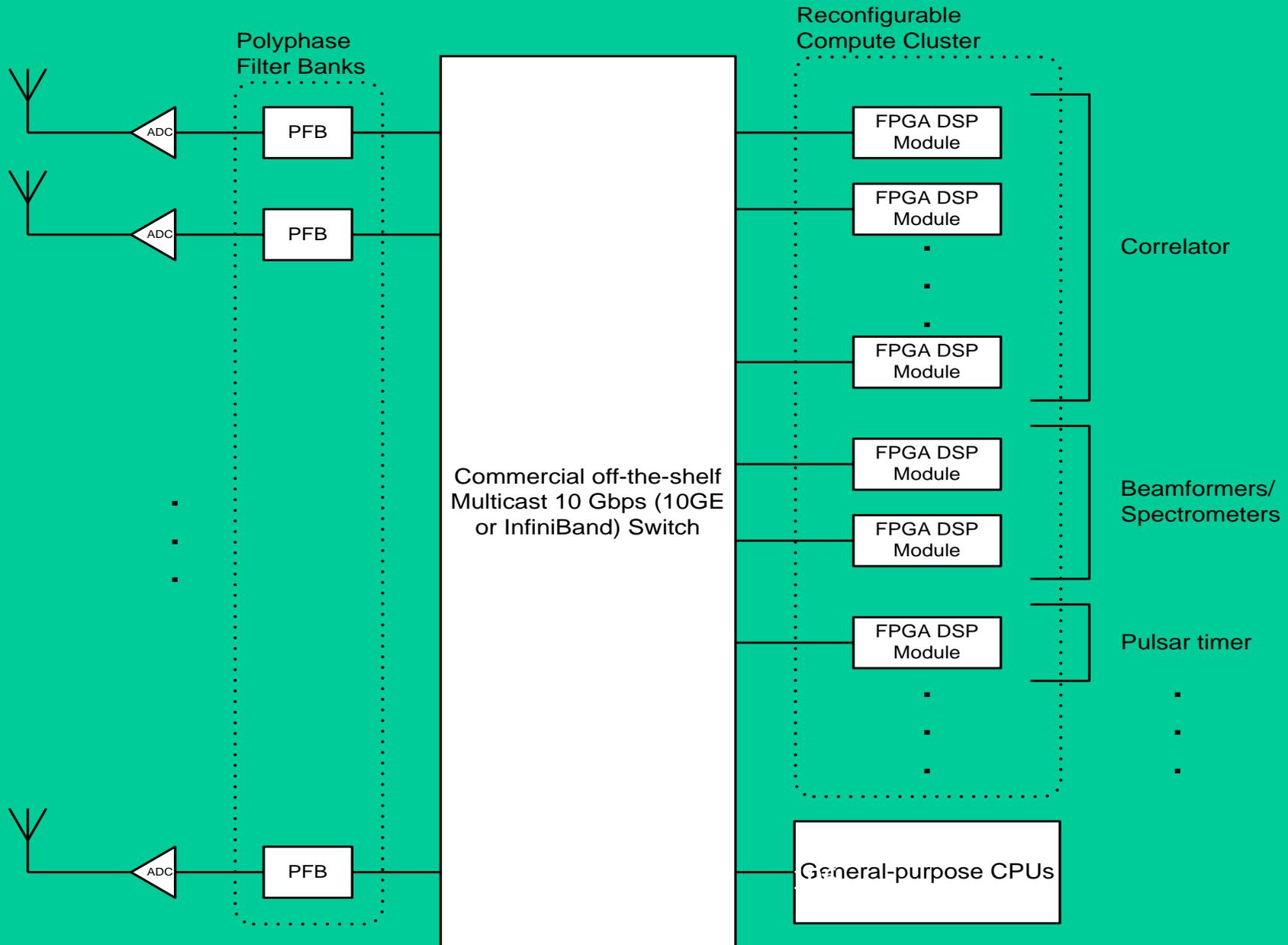
10Gbe NIC → CPU → GPU → CPU → DISK

Correlators and Beamformers

- Globally Asynchronous (like a computer cluster)
- Data is time stamped with 1 PPS at ADC
- Locally Synchronous, Globally Asynchronous
- Solve problem of correlator/beamformer interconnect problem by using 10 Gbe switches (for both interconnect and fast readout)
- No need for high density complex boards
- Use Fifo's to align data before correlation or beamforming...

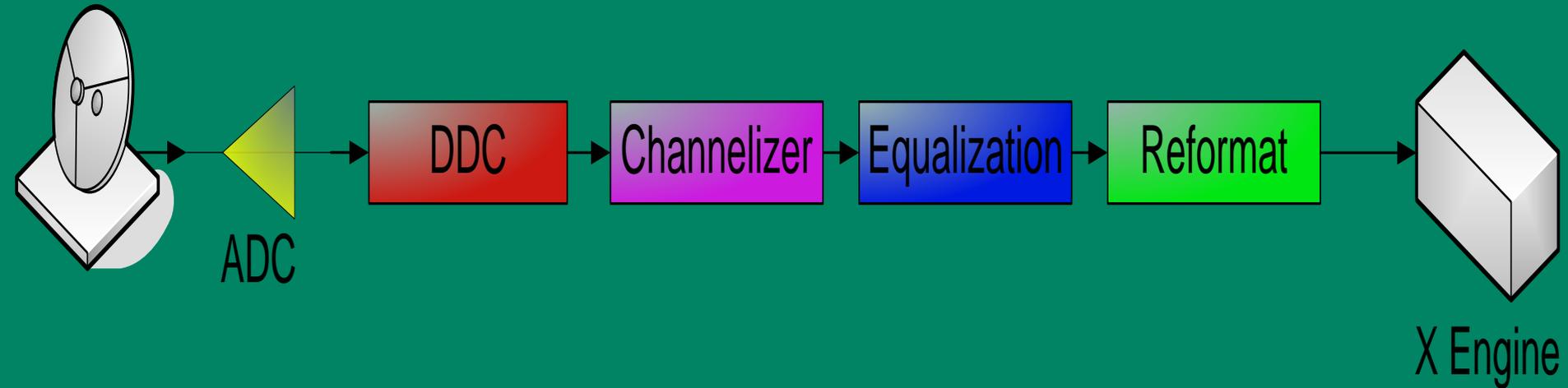
Beowulf Cluster Like General Purpose Architecture

Dynamic Allocation of Resources, need not be FPGA based

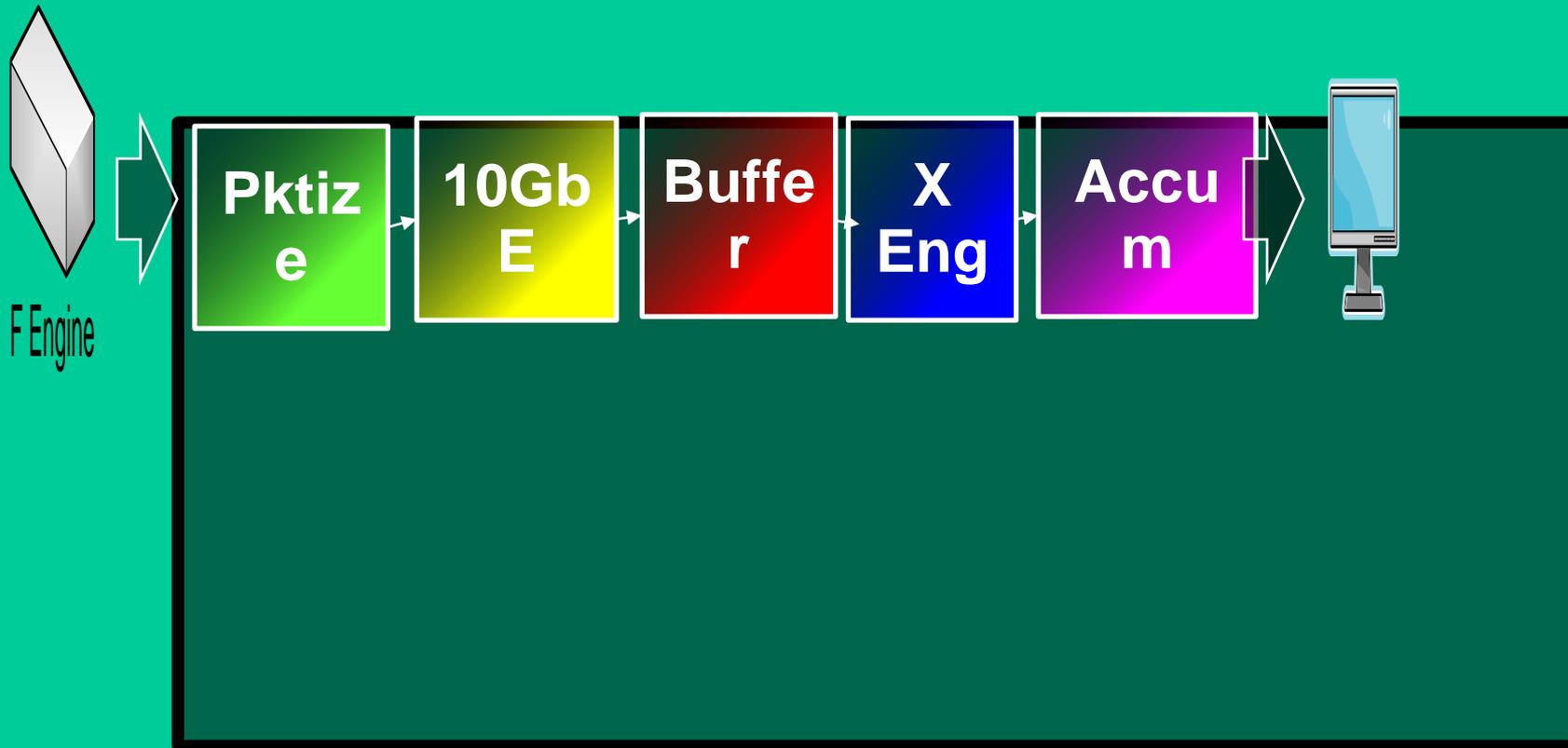


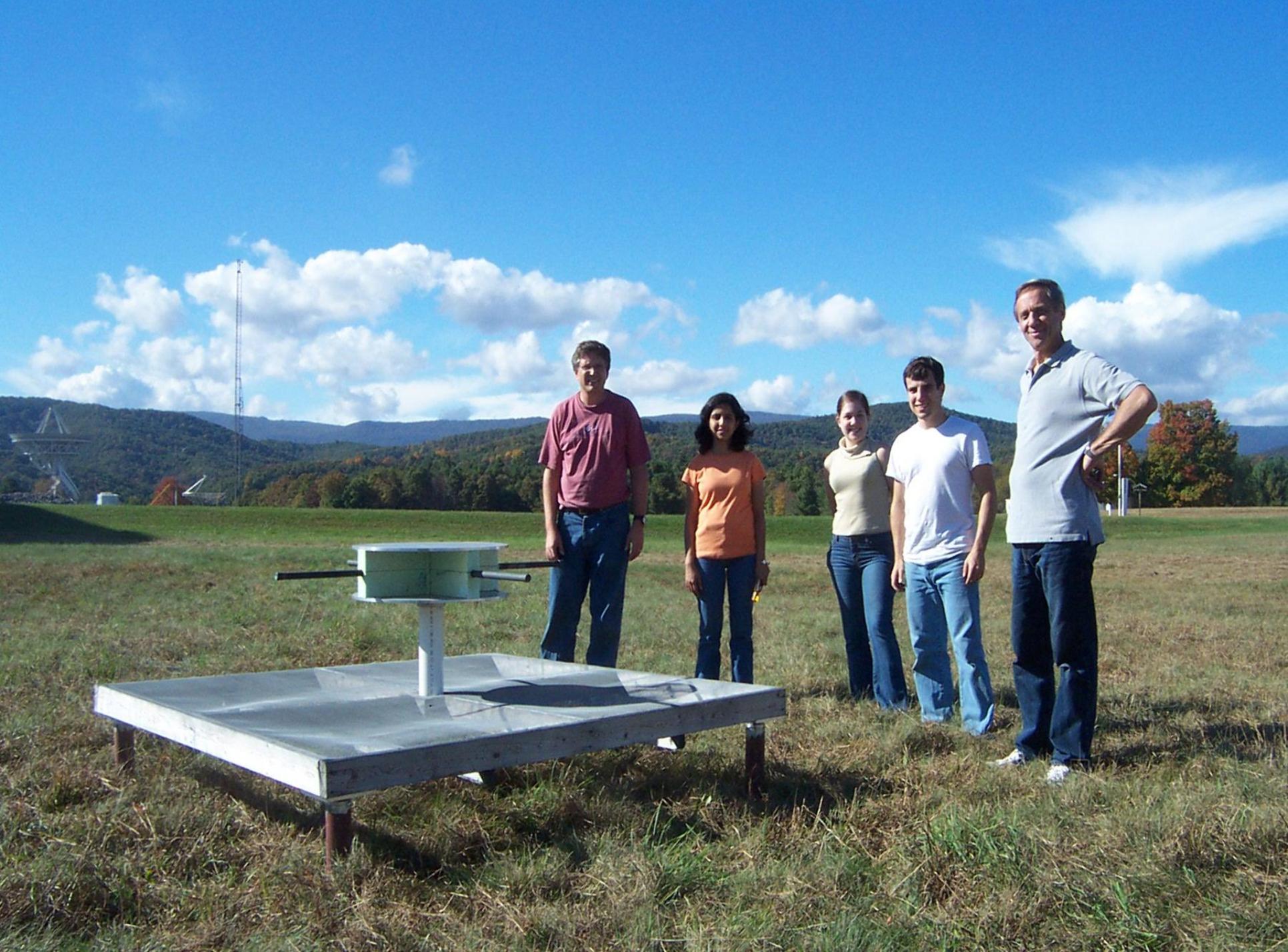
F Engine Overview

- Dual polarization design



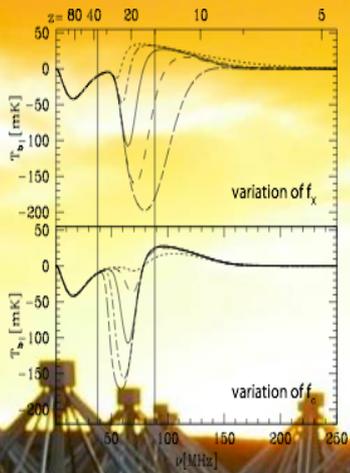
X Engine Overview







New Mexico, Owens Valley



HERA Array 547 x 15 meter dishes

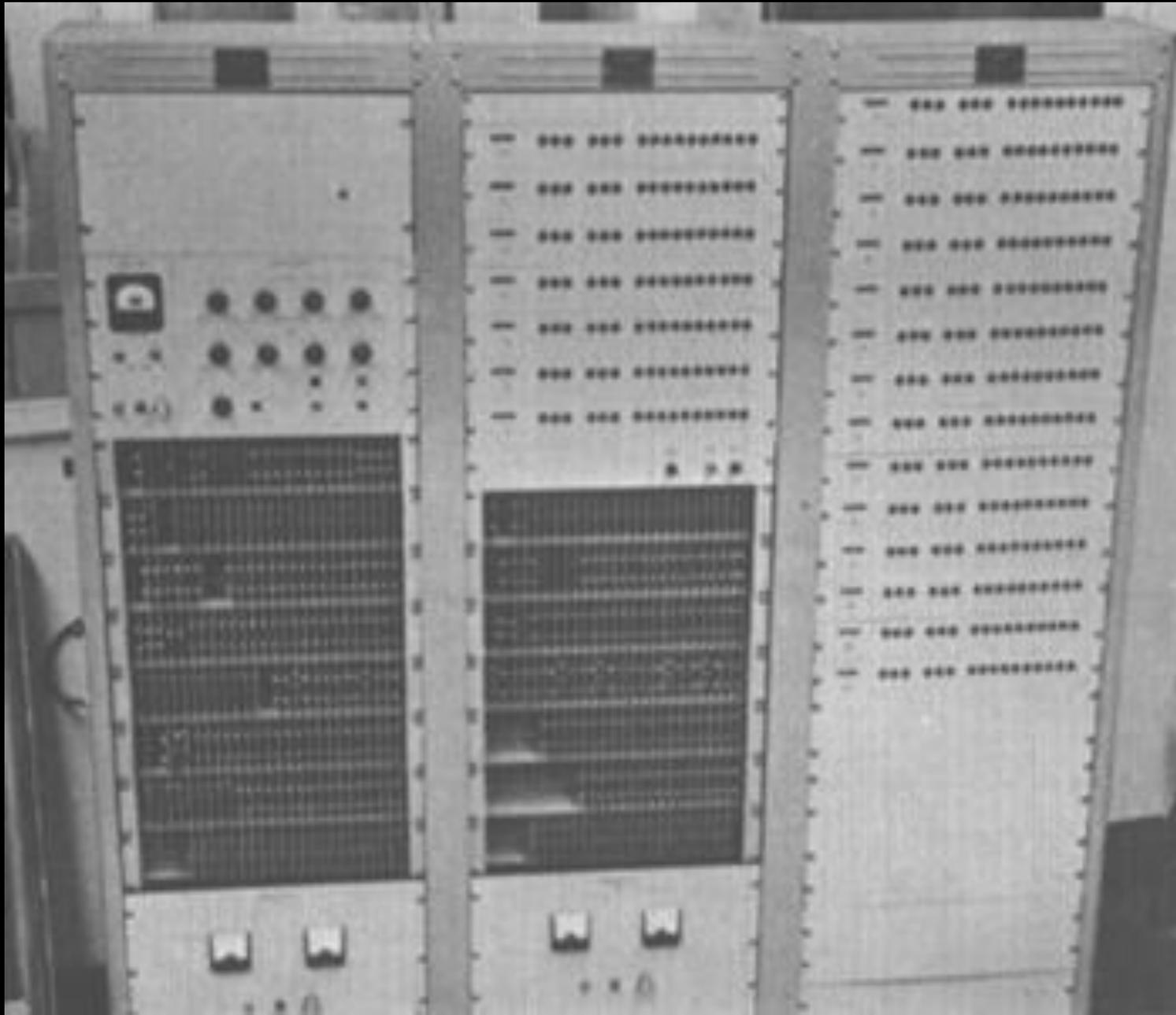


1960 – First Radio Astronomy Digital Correlator

21 lags
300kHz clock
discrete transistors

\$19,000

Sandy
Weinreb



Correlator processing power



source: Arnold van Ardenne

Ray Escoffier

“With correlator performance having gone up by a factor of 922,000 over the last 30 years, its only fair that correlator design engineers' salaries should have gone up by a similar factor!!”

Correlator Projects

- Communications - \$100M/SKA

RDMA 10/40Gbe NIC to GPU

CWDM, DWDM, 40/100Gbe, BIG Switches

- Help us design HERA Correlator

(600 antenna, 250 MHz, South Africa)

- New Platforms – Intel Phi?, FGPA, ASIC?, Next Gen GPU, CPU Arrays,
- Optimize Code (FPGA, GPU...)
- Design Study (power(t), cost(t)...)
- New Architectures (Upgradable, Scalable...)
- Build a Prototype Correlator and improve it

CASPER the Friendly GHOST

- Group Helping Open-source Signal-processing Technology (GHOST?)
 - Goal to help develop signal processing instrumentation and libraries for the community.
 - Open source hardware, gateware, and software.
 - Mail list for collaborators helping each other
 - Provide training and tutorials
 - Promote Collaboration

Tutorials (Monika Obracka, Jack Hickish, et al)

Introduction to Simulink and Roach (blink an LED)

Using 10 Gbit Ethernet

Spectrometer (400MHz, 2k channels)

Correlator (4 input, 400MHz, 1k channels)

Heterogeneous Computing ADC→ROACH→CPU/GPU

Intro to embedding Verilog/VHDL in Simulink

Yellow Block Creation

Invitation to Tenth Annual CASPER Workshop

Berkeley

Monday June 9 through Friday June 13, 2014

morning: talks

afternoon: lab training, tutorials, working groups,
get help designing an instrument....