OPENFABRICS ALLIANCE

10TH ANNUAL INTERNATIONAL DEVELOPER WORKSHOP

PANEL Session : The Future of I/O from a CPU Architecture Perspective

#OFADevWorkshop

Session Participants

- Scot Schultz, Director HPC and Technical Computing, Mellanox – Moderator
- Panelists:
- AMD : Brad Benton, PMTS, AMD Research
- CRAY : Paul Grun - Storage I/O and Interconnect Architecture
- Intel : Bill Magro, Director Technical Computing Software Solutions

PLEASE - Audience participation is encouraged!

Goals

- The goal of the panel is to have thought provoking discussion around the issues and potential solutions or needed capabilities to improve I/O performance from the CPU architecture
- Introduce ideas on how we should be thinking about I/O going forward?
- Identify what types of trends today might drive issues to be solved at higher scale

Reminder :

This is not a technology roadmap or product discussion

Trends that demand greater IO

- Consistent and constant increase of data
  - Storage requirements
  - Emerging HPC Data Analytics
- The ever-increasing amount of compute cores
  - GPUs
  - PHIs
- Storage technologies
  - Flash other technologies; PCI-Express and DIMM based
  - TCP/IP Storage; i.e. Seagate Kinetic
  - RDMA
  - Storage drives to do the heavy storage lifting (reading, writing, deleting and mirroring objects) in the background
- Network resources
  - How will processes and threads communicate more effectively / efficiently as we move to Exascale?
  - Greater demand for network bandwidth and capabilities

Topics to get us started…

- When is it time for application offloading from the CPU to the I/O device…
- Future for I/O? NICs, GPUs, Storage Adapters ; tighter integration benefits / downsides…
- What's beyond SRIOV/MRIOV for virtualization of I/O for QOS?
- When does it make more sense to bring compute closer to the data…
- Unifying programming models for I/O and CPU virtualization and coherency…
- Future improvements to the bottlenecks with Big Data?

Thank You

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