





## SHMEM/PGAS Developer Community Feedback for OFI Working Group

#OFADevWorkshop

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# Outline



- Brief SHMEM and PGAS intro
- Feedback from developers concerning API requirements
  - Endpoint considerations
  - Memory registration
  - Remote memory references
  - Collectives
  - Active messages
- On going work

# (Open)SHMEM





- Library based one-sided program model
- All ranks (PEs) in the job run the same program (SPMD) Data segments
- Only objects in symmetric regions data segment(s), symmetric heap – are guaranteed to be remotely accessible
- Various vendor specific variations/extensions
- Somewhat archaic interface (think Cray T3D), being modernized as part of OpenSHMEM effort

# UPC





- Compiler based program model 'c' with extensions
- Each thread has affinity to a certain chunk of shared memory
- Objects declared as *shared* are allocated out of shared memory
- Objects can be distributed across the chunks of shared memory in various ways blocked, round robin, etc.
- Collective operations, locks, etc.
- Like MPI, evolving over time
- Thread may map to SHMEM PE rank enumeration
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Example for array X as declared below:

```
shared [3] int x[(T*3)+3]
where
T = THREADS
```

![](_page_4_Picture_0.jpeg)

- Also compiler based one-sided program model
- CoArray construct part of Fortran 2008 standard
- Like SHMEM, currently supports only SPMD model
- Address space model closer to SHMEM than UPC
- But there is a significant complication with Fortran 2008 (and likely in future versions of UPC). Basically with Fortran 2008 not a clean separation between "shared" and "private" address spaces.

![](_page_5_Picture_0.jpeg)

# **Community Feedback**

### SHMEM/PGAS API Requirements – caveats and disclaimers

![](_page_6_Picture_1.jpeg)

- Assume significant degree of overlap with needs of MPI community, e.g.
  - Similar needs with respect to supporting fork
  - Similar needs concerning *munmap* if memory registration/deregistration needs to be managed explicitly by the SHMEM/PGAS runtime
- What are covered here are API requirements more particular to SHMEM/PGAS and similar one-sided program models
- As with MPI there are differences of opinion how best to implement runtimes to support these program models – some preferring active message style models, possibly with some RDMA offload – while others prefer a more direct-on-top-of-rdma primitives approach

# **API Endpoint Considerations**

![](_page_7_Picture_1.jpeg)

- Endpoint memory usage needs to be scalable
- Low overhead mechanism for enumeration of endpoints, i.e. "ranks" rather than lids, etc.
- It would be great to have connectionless (yet reliable)-style endpoints
- If connected-style endpoints are the only choice, methods to do both on-demand and full-wire up efficiently would be great
- API that supports "thread hot" thread safety model for endpoints.

## Memory Registration API Requirements (1)

![](_page_8_Picture_1.jpeg)

- Necessary evil?
  - Some say yes if needed for good performance
- Scalability of memory registration is a very important property
  - API should be designed to allow for cases where only local memory registration info is required to access remote memory
  - Does this lead to security issues? Have to have some protection mechanism.
- An idea let application supply "r\_key" values to use
- Growable (both down and up) registrations would also be useful (mmap example)

# Memory Registration API Requirements (2)

![](_page_9_Picture_1.jpeg)

- On-demand paging option requirements
  - Want flexibility to do on-demand paging when requested, but may also want "pinned" pages method, specified by application
  - PGAS compiler has to have control of memory allocation to avoid needing this but often compiler does have control of heap allocator, etc.
  - Fortran 2008, possible future versions of UPC may still find this useful
  - Maybe also be helpful for library based one-sided models, esp. if specifications relax current restrictions on what memory is remotely accessible become more relaxed
- Fortran 2008 (CoArray) in particular could benefit from ability to register large amounts of virtual memory that may be only sparsely populated

# Small remote memory reference API requirements – perf and ops

![](_page_10_Picture_1.jpeg)

- PGAS compilers implemented directly on top of native RDMA functionality need an API that can deliver high performance for small non-blocking PUTs (stores) and GETs (loads). Typical remote memory accesses much smaller than for MPI programs and many more of them
- Atomic memory ops are important
- Put with various completion notification mechanisms more on this in a later slide
- Small *partially* blocking put requirement (till safe to reuse local buffer)
  - Shmem on top of portals4/non-blocking puts semantics example cost of implementing partially blocking on top of non-blocking?

### Small remote memory reference API requirements - ordering

![](_page_11_Picture_1.jpeg)

PGAS compilers in particular have a special ordering requirement: Need to be able to correctly handle WAW, WAR, and RAW from a given initiator to a given target address:

![](_page_11_Figure_3.jpeg)

Problem is one getting correctness while maintaining performance. If X != Y, then no need to order operations, only if X == Y is ordering necessary. For Cray compiler, its been found for most PGAS apps X != Y is the far more common case.

# Small remote memory reference API requirements – Atomic memory ops

- Rich set of AMOs also useful need more than FADD and CSWAP.
- Multi-element AMOs for active message support, etc.
- Nice to have AMOs that can support MCS lock algorithm at scale implies possibly needing 128 bit AMOs
- At least two kinds of AMO performance characteristics:
  - Low latency but reliable (either fail or succeed, result being reported back to initiator). This allows use of locks, queues, etc. without giving up on resilience to transient network errors.
  - "At memory" computation, but only need a good enough answer. Throughput more important than reliability. Example is GUPS.
- 32/16 bit granularity ops would be useful in addition to 64 bit and possibly 128 bit.
- AMO cache (on NIC) coherency issues may need functionality in any API for this.

![](_page_13_Picture_0.jpeg)

![](_page_13_Picture_1.jpeg)

- Lightweight completion notification is very desirable, especially for PUTs.
  - Put with flag (delivered at target after payload)
  - Counter-like completion mechanism at target
  - At initiator side want notification of local completion (safe to reuse buffer), and global completion (safe to tell another process it can access the data at the target node).
- Ideally allow for batching of groups of PUT/GET requests with a single completion notification at the initiator.
- Get completion information at target of the get operation:
  - Data in the get buffer has been read and heading over the wire, i.e. target can reuse the buffer
  - Data has arrived in initiator's memory

![](_page_14_Picture_0.jpeg)

![](_page_14_Picture_1.jpeg)

- Option for fences between RDMA transactions already there?
- Per transfer network ordering options would be great
- For large RDMA writes piggyback message data (more than 32 bits of imm data) coming along with bulk data – Gasnet request – handler invocation

![](_page_15_Picture_0.jpeg)

![](_page_15_Picture_1.jpeg)

- Would be nice to not have to reinvent the wheel for multiple, often concurrently used program models, e.g. app using SHMEM and MPI
  - A lower level common interface for frequently used collective operations – barrier, reductions, coalesce (allgather), alltoall
  - Flat would be better, not have to do special on-node (within a cache coherent domain) operations within the SHMEM/PGAS implementation

### Active Message Support

![](_page_16_Picture_1.jpeg)

- Two general types of uses
  - Lower performance need for RPC-like capabilities implied by some types of operations, e.g. upc\_global\_alloc
  - Higher performance needed for PGAS languages implemented using an Active Message paradigm, as well as other active message based program models like Charm++
- API should support sending of requests to pre-initialized queues, for which the target has registered callback functions to process the data sent from initiator. Payload can be restricted to small size ~256 bytes or less.
- Initiator of message should get response back that message has arrived, optionally that message has been consumed by callback function
- Implementation needs to be able to handle transient network errors, message is delivered once and only once to target
- Some applications may require ordering of messages from a given initiator to given target, would be good to be able to specify this at queue initialization.
- Flow control is important.

![](_page_17_Picture_0.jpeg)

![](_page_17_Picture_1.jpeg)

- Working with DOE Office of Science Co-design teams to collect additional, future requirements particularly for new program models like Legion.
- Soliciting focused input from Charm++, PAMI end users, etc.

# References

![](_page_18_Picture_1.jpeg)

- <u>http://openshmem.org/</u>
- <u>BM Parallel Environment Runtime Edition Version 1 Release 2:</u> <u>PAMI Programming Guide (SA23-2273-03)</u>
- Using the GNI and DMAPP APIs
- <u>http://www.cs.sandia.gov/Portals/portals4-spec.html</u>
- <u>http://www.openfabrics.org/downloads/OFWG/</u>

![](_page_19_Picture_0.jpeg)

### **Thank You**

![](_page_19_Picture_2.jpeg)

![](_page_19_Picture_3.jpeg)

# This material was assembled with help of the following organizations/people

![](_page_20_Picture_1.jpeg)

#### Los Alamos National Lab

Latchesar lonkov

**Ginger Young** 

#### Oak Ridge National Lab

Steve Poole

Pavel Shamis

#### Sandia National Lab

Brian Barrett

#### Intel

David Addison Charles Archer Sayantan Sur

#### Mellanox

Liran Liss

#### Cray

Monika ten Bruggencate Howard Pritchard (scribe)

Input was also obtained from Paul Hargrove (LBL) and Jeff Hammond (ANL), and others.

# UPC/Fortran 2008(2)

![](_page_21_Picture_1.jpeg)

![](_page_21_Figure_2.jpeg)

This is not currently a legal UPC code example, but Fortran 2008 equivalent is. Just did not want to use Fortran for example.

# Different Views of PGAS – implementing and using

![](_page_22_Picture_1.jpeg)

Active Message Based Implementations

implementer viewpoints

Pure (almost) onesided implementations

Productivity more important than performance

user viewpoints

Expect SHMEM, etc. to beat MPI on performance

Want to use SHMEM, etc. inside MPI app for performance reasons

![](_page_23_Picture_0.jpeg)

### **Backup Material**

# (Open)SHMEM - example

![](_page_24_Picture_1.jpeg)

![](_page_24_Figure_2.jpeg)

```
return(0);
```

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# UPC

![](_page_25_Picture_1.jpeg)

![](_page_25_Figure_2.jpeg)

- Compiler based program model 'c' with extensions
- Each thread (PE in SHMEM model) has affinity to a certain chunk of shared memory
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# Small remote memory reference API requirements – AMO survey

| Operation   | IBM BG/Q | Cray XC  | Quadrics SHMEM | IB |
|-------------|----------|----------|----------------|----|
| swap        | x        | Х        | x              | -  |
| comp & swap | x        | x        | x              | х  |
| masked swap | x        | x (AFAX) | x              | -  |
| add         | x        | x        | x              | х  |
| bitwise or  | x        | x        | -              | -  |
| bitwise and | x        | x        | -              | -  |
| comp & or   | x        | -        | -              | -  |
| comp & add  | x        | -        | -              | -  |
| comp & or   | x        | -        | -              | -  |
| comp & and  | x        | -        | -              | -  |
| comp & xor  | x        | -        | -              | -  |
| min         | -        | x        | -              | -  |
| max         | -        | х        | -              | -  |

### Small remote memory reference API requirements - ordering

![](_page_27_Picture_1.jpeg)

app knows g\_idx has no overlap

#### PGAS compilers in particular have a special ordering requirement:

Many PGAS compilers can benefit greatly from hardware which provides protection against WAW, WAR, and RAW hazards for remote memory references from a given initiator to a given target and address in the target's address space.

```
between different threads, but
                                                                      possible repeat of indices for one
                                                                      thread, so no need for locks, etc.
#include <upc relaxed.h>
                                                                      in update loop
void update shared array(shared long *g array, long *local data, int *g idx, int nupdates)
   int i;
                                                              Problem for compiler is here.
   for (i=0;i<nupdates;i++) {</pre>
       g array[g idx[i]] += local data[i];
                                                              What if for some n,m it is the
   }
                                                              case that g_idx[n] ==
  upc barrier(0);
                                                              g_idx[m]. See notes.
   if (MYTHREAD == 0) {
       printf("Done with work\n");
}
```